Reducing clean cell loss rate in wireless ATM networks

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Abstract. In wireless asynchronous transfer mode (ATM) networks, the bit error rate is high and burst errors may occur in transmission due to jamming and fading. When single-bit error occurs in cell header, it can be easily corrected by the CRC-8 code in the HEC (Header Error Correction) field. However, HEC can not recover the cells with burst errors, and they will be lost or mis-routed accordingly. A strategy to spread each bit of a header field over the entire data field has been proposed to reduce the cell loss probability in wireless ATM networks. In such method, most burst errors are transformed into single-bit errors in header and the HEC is able to recover it. Intuitively, each corrected cell has a higher probability to contain incorrect payload due to burst errors. When network becomes congested, these dirty cells should be dropped first to reduce the number of error cells received by receiver. Meanwhile, the number of retransmitted cells is also reduced. In this paper, the cell payload error probability of a corrected cell is analyzed. A simple cell priority swapping mechanism and the cell discarding strategy are also introduced to reduce the clean cell loss rate on wireless ATM networks. To precisely recognize dirty cells, an efficient hybrid data/header interleaving strategy is proposed. The performance of proposed strategies are investigated by simulation. The simulation results show that the proposed strategies substantially reducing the clean cell loss rate.

Keywords: HEC, interleaving, wireless ATM, HEC

1. Introduction

Wireless Asynchronous Transfer Mode (ATM) systems have been proposed for future broadband multimedia personal communication [1,2,5]. In a wireless ATM network, the ATM cells are transmitted between a central station and several user radio modules in radio frame, as shown in Fig. 1. Due to jamming and fading, the bit error rate is high and burst errors may occur occasionally. When single-bit error occurs in header, the CRC-8 code in the HEC (Header Error Correction) field is able to correct it easily. However, HEC can not recover the burst errors in cells, and these cells will be lost or mis-routed accordingly. The ATM cell format is shown in Fig. 2. For solving this problem, an interleaving method [3] was proposed to reduce the cell loss and cell insertion probabilities. The cell interleaving method distributes all header bits within a cell. As a result, most burst errors are transformed into single-bit errors in header and they also can be corrected by the HEC field. Therefore, the cell loss rate is further reduced.

Since the HEC only checks and corrects the header information, a corrected cell has a higher probability to contain incorrect payload within it. In this paper, the corrected cells are denoted as *dirty* cells. As the network becomes congestion, the dirty cells are the candidates to be blocked or dropped. This can be done by managing the Cell Loss Priority (CLP) bit in the ATM cell header [5]. Recall that the CLP bit in the ATM cell header indicates whether a cell is high priority (CLP = 0) or low priority (CLP = 1). The network can use selective cell discarding mechanism to ensure the guaranteed QoS (Quality of Service) for certain traffic parameters for the CLP = 0 cell flow to achieve the performance of a connection. To decrease the number of error cells received in the destination, a cell discarding strategy was proposed [6]. In this strategy, the CLP bits of a dirty cell with high priority and a clean cell with low priority will be changed. When network is congested, the nonconforming cells (CLP = 1) will be dropped. Besides, it will drop the dirty cells before dropping the clean cells with the same priority. Therefore, in this strategy, lots of dirty cells will be dropped in network congestion and the cell loss probability of the QoS parameter is still satisfied.

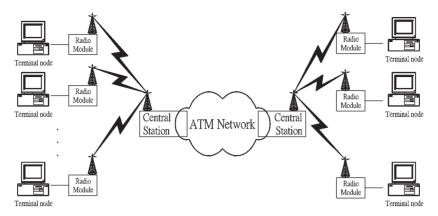


Fig. 1. The wireless ATM network.

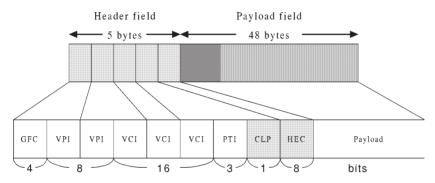


Fig. 2. ATM cell format.

In this paper, we employ the interleaving method [3] to find out which cell may contain incorrect payload (i.e., dirty cell). According to this information, the priority of each cell may be changed during transmission. Based on this concept, a cell discarding strategy is proposed to select a proper cell to drop.

The rest of this paper is organized as follows. The employed interleaving method is addressed in Section 2. In Section 3, the cell payload error probability of a corrected cell is analyzed. The priority mechanism and the cell discarding strategy are described in Section 4. In Section 5, an enhanced data/header interleaving strategy is introduced. The cell payload error probability of a corrected cell with this strategy is also analyzed. The simulation model and results are reported in Section 6. Conclusion remarks are given in Section 7.

2. Method of interleaving

Since the burst errors in header can not be corrected by the HEC, a simple interleaving header and data bits has been proposed for wireless ATM networks. The 40 header bits are distributed into a cell. That is, the number of data bits inserted into two adjacent header bits is $9 (\lfloor 48/5 \rfloor = 9)$. The cell format of an interleaved cell is shown in Fig. 3. Based on this technique, burst errors in header are spread out as isolated random errors in the header field of the cell. In other words, most burst errors are transformed into single-bit errors. Since these single-bit errors in the header are easily corrected by HEC, this interleaving can effectively reduce the cell loss and cell insertion probabilities. We note that this method is effective for burst errors shorter than 11 bits.

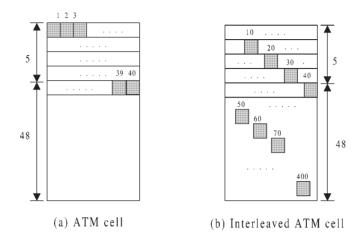


Fig. 3. The cell format of interleaving method.

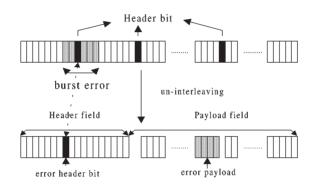


Fig. 4. The ATM cell format after de-interleaving.

3. Analysis of cell payload error probability

Though a cell may be survived by the interleaving method, the unprotected payload in it may be incorrect due to burst errors. In this section, we give analyses of the cell payload error probability (*CEP*) with interleaving method. Consider a cell is transmitted from user radio station to a central station, the burst error is occurred. If only one header bit is error in the cell, it will survive after de-interleaving and correcting as shown in Fig. 4. Let *BER* and p_i denote as the single error bit probability and the *i*-bit burst error occurrence probability. To keep the eventual bit error rate the same, the 2-bit burst error occurrence rate is assume to be one half of single error probability ($p_2 = BER/2$). Similarly, the *n*-bit burst error occurrence rate is BER/n ($p_n = BER/n$). For simplicity to express the cell error probability in a simple equation, different burst error lengths are classified into four cases. Consider the case of burst error length varies from 2 to 10, the error probability in a recoverable cell is

$$Q_1 = C_1^{40} \times \left(\sum_{i=2}^{10} p_i^i \times i\right) \times q^{39},$$

where q is the probability of the correct bit of the cell (q = 1 - BER).

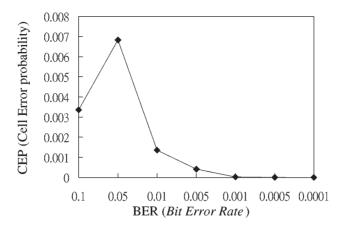


Fig. 5. The derived CEPs of employing header interleaving method under different BERs.

The error probability in a corrected cell when burst error length varies from 11 to 19 is

$$Q_2 = \left(C_1^{39} \times \left(\sum_{i=11}^{19} p_i^i \times (20 - i)\right) + C_1^1 \times \left(\sum_{i=11}^{19} p_i^i \times 10\right)\right) \times q^{39}.$$

Consider the case with burst error length varies from 20 to 25, the error probability in a recoverable cell is

$$Q_3 = C_1^1 \times \left(\sum_{i=20}^{25} p_i^i \times 10\right) \times q^{39}.$$

In the last case, the burst error length is considered from 26 to 34, the cell error probability is calculated as

$$Q_4 = C_1^1 \times \left(\sum_{i=26}^{34} p_i^i \times (35 - i)\right) \times q^{39}.$$

Thus, the total cell payload error probability can be easily obtained by the following equation: $CEP = Q_1 + Q_2 + Q_3 + Q_4$. The analyzed CEPs under different bit error rates (BERs) are shown in Fig. 5.

4. Cell discarding strategy (CDS)

For simplicity to describe the cell discarding strategy, four types of cells are classified: (1) dirty cell with low priority (*DL*); (2) dirty cell with high priority (*DH*); (3) clean cell with low priority (*CL*); (4) clean cell with high priority (*CH*). Obviously, *CH* and *DL* cells have the highest priority and the lowest priority, respectively. To provide the QoS of a connection, the specified cell loss probability should be maintained during transmission. That is, if the cell discarding strategy considers not only the cell priority but also the cell status (clean or dirty) for dropping, more clean cells will be received by the receiver. Besides, a better quality of service is provided. According to the operations of CLP bit in header field, the *CL* cells will be dropped before the *DH* cells when buffer congested. Therefore, a *CL* cell is allowed to change its priority with a *DH* cell queued in the buffer (see Fig. 6). As a result, the corresponding *CL* cell and *DH* cell will become a *CH* cell and a *DL* cell, respectively. The following cell discarding operation will scarify these dirty cells. This introduces the cell discarding strategy (CDS) for reducing the number of error cells received by destinations.

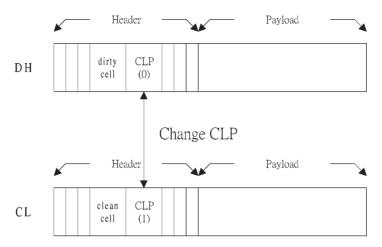


Fig. 6. Changing CLP of the DH and CL cells.

5. Data/header interleaving strategy

To avoid mis-dropping clean cells in the proposed cell discarding strategy, we propose the data/header interleaving method to precisely find out which cell is dirty or clean.

5.1. Block cells interleaving

To obtain a higher survivability, a block cells header interleaving expansion method was proposed in [4]. In this method, header bits of a number of n consecutive ATM cells are distributed into these cells. The header bits of each cells are separated by $9 \times n$ bits. Therefore, each cell has a higher probability to survive when burst length of error is longer than 10 bits. Figure 7 shows the cell format of 5 cells after performing block cells interleaving.

5.2. Data/header interleaving

Based on the multicell interleaving approach, we propose the data/header interleaving method to precisely determine which cell is dirty or clean. When a high priority dirty cell and a low priority clean cell are found accurately, their CLP bits are swapped at that moment.

The way of deciding a cell is dirty or clean is described as follows. Recall that the bit errors may occur in burst due to multi-path, jamming and fading in wireless networks. When HEC detects an error header bit, the neighbor data bits may also be incorrect at the same time. In the multicell header interleaving approach, if all data bits of one cell are spread and located on the neighbors of all header bits, any error header bit implies that this cell has a higher probability to contain incorrect payload. On the contrary, if no error occurs on all header bits during transmission, we say this cell is clean. Therefore, this method not only interleaves the header bits but also interleaves the data bits within a number of consecutive cells. This is why we call this method as data/header interleaving strategy.

For simplicity to demonstrate, five consecutive ATM cells are grouped together to perform the data/header interleaving. They are numbered from C_1 to C_5 according to the arrival sequence. That is, each time five cells arrive buffer, the first arrived cell is denoted as C_1 , and the second arrived cell is denoted as C_2 , etc. Let cells I^1 , I^2 , I^3 , I^4 , and I^5 denote as the derived cells after performing data/header interleaving on cells C_1 , C_2 , C_3 , C_4 and C_5 . The total header bits ($40 \times 5 = 200$) in group are equally distributed into these five cells. Obviously, each cell in the group contains 8 header bits from each cell. Similarly, the number of data bits inserted into two adjacent header bits is 9 also. Let i be the index of cell in a group ($1 \le i \le 5$), and a is the index of the header bit in a cell

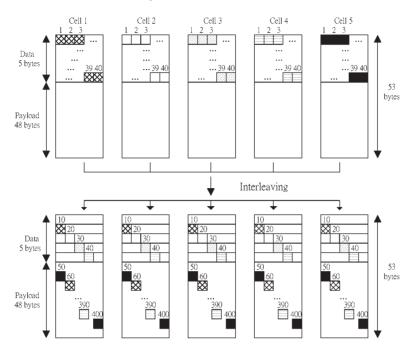


Fig. 7. The cell format of block cells interleaving (n = 5).

 $(1 \le a \le 40)$. The assigned position $(C_i(H_a))$ of the a-th header bit in cell C_i can be easily determined by the following equation:

$$C_{i}(H_{a}) = \begin{cases} I_{[i+5(a\%8-1)]\times10}^{\lceil a/8 \rceil}, & a\%8 \neq 0, \\ I_{(i+35)\times10}^{\lceil a/8 \rceil}, & \text{otherwise,} \end{cases}$$

where I_y^x stands for the y-th bit location in the I^x cell after performing data/header interleaving.

For the sake of improving the ability to find the dirty or clean cell, the data bits of each cell are also interleaved in a particular way. The data bits of cell C_1 are distributed as the neighbors of all header bits. The data bits of cell C_2 (C_i) are located as the neighbors of all data bits of C_1 (C_{i-1}). Let $C_i(D_b)$ denote the assigned position of the bth data bit ($1 \le b \le 384$) in cell C_i . For cells C_1 , C_2 , C_3 , and C_4 , the assigned position $C_i(D_b)$ can be easily derived by the following equation:

$$C_i(D_b) = I_{[5+(\lfloor (b-1)/2 \rfloor \%40) \times 10] + (i-5)^{b\%2}}^{\lceil \lceil b/2 \rceil / 40 \rceil}.$$

Since the data bits of the last cell C_5 are not assigned regularly, two different conditions are considered. When $1 \leq \lceil b/64 \rceil \leq 4$, we have

$$C_i(D_b) = \begin{cases} I_{5+(b-1)\times 10}^{\lceil b/64 \rceil}, & 0 \leqslant (b-1)\% 64 \leqslant 39, \\ I_{400+(b-40)}^{\lceil b/64 \rceil}, & 40 \leqslant (b-1)\% 64 \leqslant 63. \end{cases}$$

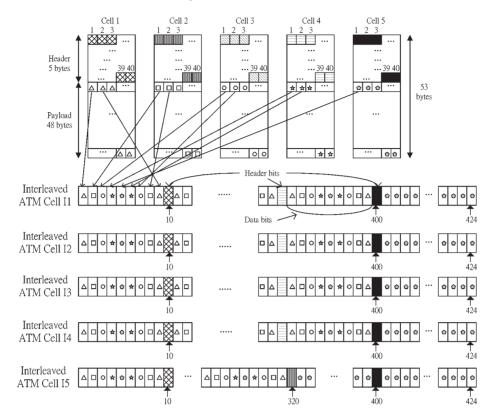


Fig. 8. The bit assignment of the data/header interleaving strategy.

Other data bits located from 257 and 384, the corresponding positions are assigned as follows.

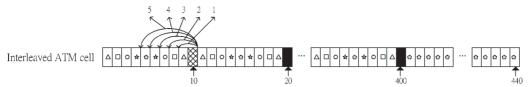
$$C_i(D_b) = \begin{cases} I_{5+\lceil (b-256)-1 \rceil \times 10}^5, & 257 \leqslant b \leqslant 288, \\ I_{321+(\lceil (b-288)/9 \rceil -1) \times 10+\lceil (b-288)-1 \rceil \% 9}^5, & 289 \leqslant b \leqslant 360, \\ I_{400+(b-40)}^5, & 361 \leqslant b \leqslant 384. \end{cases}$$

The bit assignment of the data/header interleaving strategy is shown in Fig. 8. We note that each time receiver receives five interleaved cells, the distributed header and data bits must be rearranged into the original cell format. This operation can be easily done by the above equations.

5.3. Analysis of cell payload error probability

In this section, we analyze the cell payload error probability (CEP) with data/header interleaving method. Considering the case of error is detected by the HEC field while transmitting cells from user radio station to central station. According to the data interleaving approach, if the error is 2-bit burst error, the cell C_1 must contain incorrect data. Also, if 3-bit burst error occurs, cells C_1 and C_2 are dirty accordingly. It is clear that when 6-bit burst occurs, all cells are dirty (see Fig. 9).

As mentioned above, let BER and p_i denote as the single error bit probability and the i-bit burst error occurrence probability. To keep the eventual bit error rate the same, the 2-bit burst error occurrence rate is assume to be one half



Case 1: The burst length is 2, the cell C_1 contains error payload.

Case 2: The burst length is 3, the cell C_2 contains error payload.

Case 3: The burst length is 4, the cell C_3 contains error payload.

Case 4: The burst length is 5, the cell C_4 contains error payload.

Case 5: The burst length is 6, the cell C_5 contains error payload.

Fig. 9. The way of determining the data error probability of each interleaved cell.

of single error probability ($p_2 = BER/2$). Similarly, the *n*-bit burst error occurrence rate is BER/n ($p_n = BER/n$). The probability of error only occurs on cell C_1 , say E_1 , is derived by the following equation:

$$E_1 = C_1^{187} p_2^2 \cdot q_2^{39} \times 2 + C_1^5 p_2^2 \cdot q_2^{39} \times 1 + C_1^{187} p_3^3 \cdot q_3^{39} \times 1.$$

Since the total number of data bits in cell C_1 is 384, they are located on the neighbors of 192 header bits. For simplicity to arrange the data bits, the first data bit in cell C_1 is located on the first position of interleaved cell which is shown in Fig. 9. Therefore, only one data bit neighbors the last header bit in each cell. That is, the first item in E_1 is the probability of the 2-bit burst error which covers one of the 187 header bits. The second item is the probability of the 2-bit burst error which covers one of the 5 particular header bits. The third is the case where just 3-bit burst error covers a header bit and two adjacent data bits belong to cell C_1 . Similarly, the probability of error covers cells C_1 and C_2 can be derived by the following equation:

$$E_2 = C_1^{187} p_3^3 \cdot q_3^{39} \times 2 + C_1^5 p_3^3 \cdot q_3^{39} \times 1 + C_1^{187} p_4^4 \cdot q_4^{39} \times 2 + C_1^{187} p_5^5 \cdot q_5^{39} \times 1.$$

The probability of error covers cells C_1 , C_2 and C_3 is calculated as follows.

$$E_3 = C_1^{187} p_4^4 \cdot q_4^{39} \times 2 + C_1^5 p_4^4 \cdot q_4^{39} \times 1 + C_1^{187} p_5^5 \cdot q_5^{39} \times 2 + C_1^{187} p_6^6 \cdot q_6^{39} \times 2.$$

The probability of error covers cells C_1 , C_2 , C_3 and C_4 is

$$E_4 = C_1^{187} p_5^5 \cdot q_5^{39} \times 2 + C_1^5 p_5^5 \cdot q_5^{39} \times 1 + C_1^{187} p_6^6 \cdot q_6^{39} \times 2.$$

The probability of error covers cells C_1 , C_2 , C_3 , C_4 and C_5 is

$$E_5 = C_1^{187} p_6^6 \cdot q_6^{39} \times 2 + C_1^5 p_6^6 \cdot q_6^{39} \times 2.$$

We neglect the probability of occurring burst error length greater than 6 because it is considerably smaller than other items. Therefore, The exact cell error probability of cell C_1 is $E_1 + E_2 + E_3 + E_4 + E_5$. Similarly, the cell error probability of cell C_2 is calculated by $E_2 + E_3 + E_4 + E_5$. The cell error probabilities of each cell under different bit error rates (*BERs*) are shown in Fig. 10. From the analytic result, we can find that cell C_1 has the highest probability to contain error data. On the other hand, other cells are hardly to determine whether they are dirty or not. Therefore, when any error header bit is detected, only cell C_1 will be marked as dirty cell.

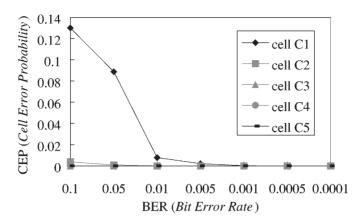
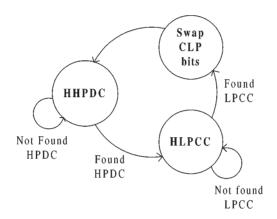


Fig. 10. The CEPs of each interleaved cell under different BERs.



where HPDC: High Priority Dirty Cell, LPCC: Low Priority Clean Cell.

Fig. 11. The state transition diagram of the data/header interleaving strategy.

5.4. Enhanced cell discarding strategy (ECDS)

To perform the cell discarding strategy, we need to find each pair of a high priority dirty cell and a low priority clean cell. That is, the cells assignment in each group is necessary to be scheduled. For example, if we are looking for a high priority dirty cell, a cell with high priority in the group should be assigned (mapped) to be cell C_1 . As soon as a dirty cell with high priority is found, the interleaving strategy will try to find a clean cell with low priority. To do this, two states are designed for deciding which kind of cell should be assigned to cell C_1 . State **HHPDC** is responsible for hunting high priority dirty cell and state **HLPCC** is looking for the low priority clean cell. Initially, ATM switch states in the **HHPDC** state. Each time a high priority dirty cell is found, it enters to the **HLPCC** state. In the **HLPCC** state, it keeps trying to find a clean cell with low priority. If the cell is detected, the CLP bits of these two cells are swapped and the ATM switch returns to the **HHPDC** state. We note that the swapping operation is done only when these two cells are still queued in a same buffer. The state transition diagram is shown in Fig. 11.

6. Simulation model and simulation results

The performance of proposed data/header interleaving and the cell discarding strategy was investigated by simulation. The simulation model is shown in Fig. 12. In Fig. 12, sources A and B want to transmit data to station C. The traffic arrival rates in source A (B) is a Poisson distribution with a mean λ_A (λ_B). To investigate the effect of proposed strategy, only source A is mobile station and the transmitted cells from it have a chance to be dirty cells or low priority cells. Contrarily, sources B only generates the clean cells with high priority to cause the network congested. Besides, there are N ATM switches are considered between stations A and C. To investigate the effect of proposed strategy, the ratio of the number of dropped dirty cells (RDD) and the total number of dropped cells are measured. Figure 13 shows the number of changing CLP between DH and CL cells under different CEPs when N=3, N=4, N=5, N=6. We can see that a dirty cell with CLP = 0 when N=6 will have a better chance to change its CLP with a clear cell with CLP = 1. That is, the no. of dropped dirty cells in the case of N=6 will

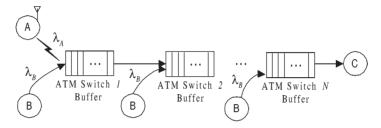


Fig. 12. The state transition diagram of the data/header interleaving strategy.

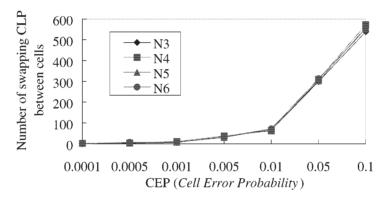


Fig. 13. The number of swapped CLP between cells under different CEPs.

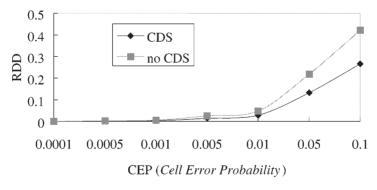


Fig. 14. The obtained *RDD*s under different *CEP*s when N=3.

be higher than that of N=3, 4, 5. Figure 14 shows the obtained *RDD*s by the proposed ECDS and the original cell discarding mechanism when N=3, $\lambda_A=0.5$ and $\lambda_B=0.2$. We note that, in this case, the total network load excesses the entire network bandwidth ($\lambda_A+\lambda_B\times N=1.1$). In Fig. 14, we can see that the obtained *RDD* by the ECDS is smaller than that of original cell discarding mechanism under different cell error probabilities.

7. Conclusion

In this paper, we introduced a data/header interleaving strategy to find out the cells with error payload and to drop them when congestion occurs in wireless ATM networks. The proposed strategy first spreads each header bit over the whole data field to reduce the cell loss probability. Secondly, it assigns the data bits of one cell to the neighbors of all header bits to determine whether this cell is clean or not. The cell error probability of a corrected cell is analyzed and the simulation results show that the proposed strategy substantially improves the clean cell loss rate.

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