# Digital Compensation for MASH Sigma Delta Modulators using H-infinity Approach

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***Abstract*—This paper presents a new digital compensation scheme for MASH (cascaded) sigma-delta modulators (ΣΔMs) with 1-bit quantizer. The compensation scheme is designed based on the well-known internal model principle and H-infinity control theory. For numerical illustration, we concentrate on a MASH 2-1 ΣΔM architecture for low and middle frequencies applications. Comparisons between the proposed ΣΔM and the conventional one are made, which reveal that the proposed ΣΔM outperforms the conventional one in several aspects - signal-to-noise ratio (SNR), dynamic range (DR), output swing.**

***Keywords*—cascaded sigma-delta modulator, digital filter, H-infinity, dynamic range, signal-to-noise ratio.**

## I. Introduction

ΣΔ analog to digital converters (ADCs) have demonstrated to be an attractive solution for the implementation of analog-digital interfaces in systems consisting of analog and digital components. Compared to Nyquist-rate ADCs, ΣΔ architectures present a better performance in terms of resolution, speed and power consumption with more robustness against the imprecision in circuit and inherent noises [1,2,3]. There are two architectures which are frequently used for ΣΔMs: single-stage and multi-stage (or cascade or MASH) structures [4].

MASH ΣΔMs have gained popularity in the design of high performance ADCs. This is because the cascaded topology in a modulator can prevent the stability problem by pipelining several lower order single-loop modulators. Therefore, there has been incentive to develop high-order MASH ΣΔMs in order to increase noise-shaping ability. However, the well-known drawbacks of cascaded architecture are component imperfections and input range reduction which cause the performance degradation. In the case of component imperfections, the modulators are naturally subject to analog mismatch in capacitor values and finite amplifier gain. As for the input range reduction, 1-bit quantizers are usually used in the cascaded modulator, i.e. the previous stage quantization error is the next stage input, which exceeds 3.5 times the input range. Therefore, the first stage input has to be reduced and such a reduction significantly increases the effect of the electronic device noise at the input node [4].

Recently, there are some research works presenting different digital techniques for correcting errors in MASH ΣΔMs, such as adaptive filter approach [5,6], robust control approach [7,8], and the other techniques [9,10,11].

In this paper, based on the previous work of the authors [12], we focus on the design of a MASH 2-1 SDM with 1-bit quantizer. We propose to design a digital filter based on robust control theory to compensate the performance degradation due to the analog imperfection and the input range reduction, meanwhile, to improve the signal-to-noise ratio. The remainder of this paper is organized as follows. In Section II, a brief review for MASH 2-1 ΣΔMs and H-infinity control technique which will be used is provided. The design objectives of this paper are formally stated. In Section III we have proposed a new compensation scheme for the ΣΔM with analog imperfections. The main characteristic of the new architecture is that a digital filter containing an internal model is placed in a negative feedback path. The control strategies are explained. Finally, the digital filter design problem is cast in H-infinity control formulation and solved. The simulation results are presented in Section IV where a standard test signal for ΣΔMs, e.g. an in-band sinusoidal input, is used. Conclusions are provided in Section V.

## II. Preliminaries and Problem Statement

In this section, a brief introduction of the MASH 2-1 sigma-delta modulators and the H-infinity control theory are presented. Next, the robust digital filter design problem we consider is formally stated.

### *A. MASH 2-1 Sigma-Delta Modulators*

A conventional MASH 2-1 ΣΔ modulator is depicted in Fig. 1, where $H_j(z)$ ($j$=1,2,3) represent integrators; $R$ denotes the input signal; $E_i$ ($i$=1,2) represents the quantization errors; $Y$ is the output signal; $a_1$, $a_2$, $b_1$, $b_2$, and $b_3$ are path coefficients. The signal transfer function (STF) and the noise transfer function (NTF) of the MASH 2-1 modulator are defined as the transfer functions from the signals $R$, $E_1$, *and* $E_2$ to the output signal $Y$, respectively. Specifically,

$$y_{out1} = \frac{a_1 a_2 H_1 H_2}{1 + b_2 H_2 + a_2 b_1 H_1 H_2} R + \frac{1}{1 + b_2 H_2 + a_2 b_1 H_1 H_2} E_1 \quad (1)$$

$$y_{out2} = \frac{H_3}{1 + b_3 H_3} E_1 + \frac{1}{1 + b_3 H_3} E_2 \quad (2)$$



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It follows that

$$Y = \frac{a_1 a_2 H_1 H_2 Q_1}{1 + b_2 H_2 + a_2 b_1 H_1 H_2} R - \frac{Q_2}{1 + b_3 H_3} E_2$$
$$+ \left( \frac{Q_1}{1 + b_2 H_2 + a_2 b_1 H_1 H_2} - \frac{H_3 Q_2}{1 + b_3 H_3} \right) E_1$$

In order to eliminate the effects on the output $Y$ due to the quantization error $E_1$, $Q_1$ and $Q_2$ are chosen as

$$Q_1 = \frac{H_3}{1 + b_3 H_3} \ , \quad Q_2 = \frac{1}{1 + b_2 H_2 + a_2 b_1 H_1 H_2} \tag{3}$$

respectively. Thus, the output signal $Y$ becomes

$$Y = T_{YR} R + T_{YE_2} E_2$$

where $T_{YR} = \frac{a_1 a_2 H_1 H_2 Q_1}{1 + b_2 H_2 + a_2 b_1 H_1 H_2}$ , $T_{YE_2} = \frac{-Q_2}{1 + b_3 H_3}$ .

Let $S_R(\omega)$ and $S_{E_2}(\omega)$ stand for the power spectral density (PSD) of input signal $R$ and quantization error $E_2$, respectively, then the spectrum of the modulator output can be expressed by

$$S_Y(\omega) = \left| T_{YR}(\omega) \right|^2 S_R(\omega) + \left| T_{YE_2}(\omega) \right|^2 S_{E_2}(\omega)$$

It follows that the powers of $Y$ due to $R$ and $E_2$ are given respectively by

$$P_R = \int_{-f_b}^{f_b} \left| T_{YR}(f) \right|^2 S_R(f) df \cong \Delta^2 2^{2N} / 8 \tag{4}$$

$$P_{E_2} = \int_{-f_b}^{f_b} \left| T_{YE_2}(f) \right|^2 S_{E_2}(f) df \cong \frac{\Delta^2}{12} \frac{\pi^{2L}}{2L+1} \left( \frac{1}{OSR} \right)^{2L+1} \tag{5}$$

where $f_b$ represents the baseband frequency, $\Delta$ is the quantization step, $N$ is the order of the quantizer used, $L$ is the order of the modulator and $OSR$ is the oversampling rate. Then the SNR of the ΣΔ modulator is given by

$$SNR = 10 \log \left( \frac{P_R}{P_{E_2}} \right)$$
$$= 6.02N + 1.76 + 10 \log \left( \frac{2L+1}{\pi^{2L}} \right) + (20L + 10) \log (OSR) \tag{6}$$

Accordingly, the ideal SNR value of a MASH 2-1 modulator with $N$=1, $L$=2, $OSR$=256 is about 154.98 dB. But (6) is derived assuming perfect analog components. However, analog imperfections are inevitable. Two common sources of analog imperfections of a ΣΔM are finite amplifier gain and mismatch in capacitor values, which are manifested as uncertainties in the gains and poles of the integrators $H_j(z)$, $j$=1,2,3 [4,7]. The non-ideality of the integrators certainly would alter the transfer functions $T_{YR}$ and $T_{YE_2}$ , consequently affecting the SNR performance (see (4)-(6)), which makes it difficult to establish a simple relationship between the factors. Worst of all, it degrades the performance.

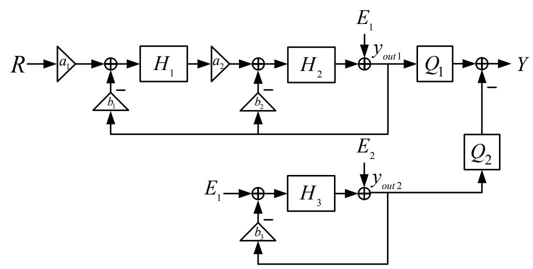


Figure 1. Conventional MASH 2-1 modulator

## B. A brief Review of the H-infinity Control Theory

H-infinity Control Theory [13] is a popular robust control technique which has been proven useful in many engineering applications. The $H_\infty$ norm of a discrete-time proper stable transfer function is defined by the formula $\|T(z)\|_\infty := \max_{\theta \in [0, 2\pi]} \left| T(e^{j\theta}) \right|$ . A popular controller synthesis paradigm is depicted in Fig. 2. The symbol $P$ denotes the discrete-time generalized plant including the nominal plant, weighting functions, etc, described by

$$P \begin{cases} x(k+1) = Ax(k) + B_1 w(k) + B_2 u(k) \\ z(k) = C_1 x(k) + D_{11} w(k) + D_{12} u(k) \\ y(k) = C_2 x(k) + D_{21} w(k) + D_{22} u(k) \end{cases}$$

where $x \in R^{n_P}$ , $w \in R^{m_w}$ , $u \in R^{m_u}$ , $z \in R^{m_z}$ , and $y \in R^{m_y}$ . $w$ represents the exogenous inputs such as disturbances, reference commands, and the auxiliary signals from the uncertainties; $z$ denotes the observed signal; the vector of measurements and control inputs are denoted by $y$ and $u$ , respectively. The symbol $K$ denotes a dynamic controller of the form

$$K \begin{cases} x_K(k+1) = A_K x_K(k) + B_K y(k) \\ u(k) = C_K x_K(k) + D_K y(k) \end{cases}$$

where $x_K \in R^{n_K}$ , to be designed.

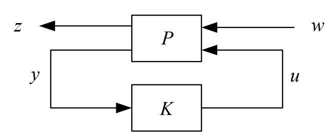


Figure 2. $P$-$K$ framework

The so called optimal $H_\infty$ control problem is to determine a stabilizing controller so that the $H_\infty$ norm of the closed-loop transfer function $T_{zw}$ is minimized. A variety of engineering problems, such as robust stability margin optimization, noise attenuation, etc, can be cast into this formulation. Specifically, when there is a parametric perturbation Δ connecting $z$ and $w$, and there exists a stabilizing controller $K$ such that $\|T_{zw}\|_\infty < \gamma$, this implies that the robust stability margin is at least $1/\gamma$, i.e., the perturbed system remains stable when the size of the perturbation is no greater than $1/\gamma$. For the problem of noise attenuation with bounded peak noise $w$, for example the quantization error, minimization of the $H_\infty$ norm of the transfer function $T_{zw}$ leads to reduction of the power of $z$ due to the noise.

### C. Goal

The goal of this paper is to design a robust digital filter to achieve high SNR and reasonable output swing against the inevitable and uncertain analog imperfections. In the following, we formulate it as a robust tracking control problem with the following control objectives:

*a)* **Robust Stability**: the closed-loop stability of the compensated ΣΔ modulator should be guaranteed for a range of parameter variations.

*b)* **Signal tracking**: the compensated ΣΔ modulator output should be able to track the test sinusoidal input.

*c)* **Noise attenuation**: the effects of the quantization errors should be attenuated.

*d)* **Output swing suppression**: The output of the critical integrator (the first one) should be suppressed such that its peak value is below the prescribed integrator saturation level so as to prevent signal clipping.

Intuitively, accomplishment of the objectives (b), (c) and (d) is supposed to be able to improve the SNR performance, which will be explained in the sequel.

## III. Robust Digital Filter Design

In this section, for illustration, a robust digital filter design is presented for a MASH 2-1 ΣΔ modulator. First, uncertainty models for the modulator with analog imperfections such as finite gain of the amplifiers and capacitor ratio mismatch are introduced. Second, the key feature of the proposed ΣΔ modulator architecture used to obtain high resolution is explained.

The proposed digital compensated system configuration is depicted in Fig. 3, where $H_i$, $i$=1,2,3 are the non-ideal (discrete-time) integrators due to the analog imperfections, and $F$ is a robust digital filter to be determined. In the following, the non-ideal integrators are modeled as

$$H_i(z) = \frac{\beta_i z^{-1}}{1-\alpha_i z^{-1}} = \frac{(1-\delta_{z_i})z^{-1}}{1-(1-\delta_{p_i})z^{-1}} \tag{7}$$

where $\delta_{z_i} \in [0,1)$ and $\delta_{p_i} \in [0,1)$ are deviations in the values of $\beta_i$ and $\alpha_i$ [7]. Note that $\delta_{p_i} = 1/A_v$ where $A_v$ denotes the finite amplifier gain [4]. Therefore, $\delta_{p_i}$ equals zero for the ideal case where $A_v$ is infinite, and is usually a small positive number (less than one) for the cases where the amplifier gain is finite.

We propose to design a digital filter that achieves the design objectives described in Section II.C. Note that $R$ and $Y$ represent the modulator input and output, respectively. For the purpose of SNR performance enhancement, the idea is to make the output $Y$ to be highly dominated by the input $R$ with respect to the quantization noises $E_1$ and $E_2$. This can roughly be approximated by requiring the error signal $e$ as small as possible. To this end, the proposed design is comprised of two actions. The first is the input signal tracking. An internal model

$$K_{IM} = \frac{T_S z^{-1}}{(1-z^{-1})^2}$$

which consists of two integrators is included in the robust filter $F$. Here $T_S$ indicates the sampling time. With this, should the closed-loop stability is guaranteed, the steady-state error $e(\infty)$ due to step or ramp type input $R$ would be completely eliminated. Further reduction of the effect of the input on $e$ is possible, which can be done by minimizing the $H_\infty$ norm of the transfer function from $R$ to $e$. Next is noise attenuation. The quantization errors that arise from the operation of the quantizers are modeled as additive bounded-peak noises $E_1$, $E_2$ [4, pp. 4]. Minimization of the $H_\infty$ norm of the transfer function from $E_1$ and $E_2$ to $e$ could make $e$ small. In total, making the error $e$ small implies that the output $Y$ keeps tracking the scaled input $a_2R$; hence the output is dominated by the input signal, which in turn implies good SNR.

To reduce the output swing of the first integrator due to the quantization errors, the idea is to minimize its contribution to the signal $u_1$ in the power sense; hence the power propagating through the first integrator is reduced. This can be done by designing a filter to minimize the $H_\infty$ norm of the transfer function from $E_1$ and $E_2$ to $u_1$. Similarly, the $H_\infty$ norm of the transfer function $T_{u_1R}$ is also to be minimized. For better loop characteristics, the weighing function $W$ is introduced; see e.g., [13] for the details of the loop-shaping technique. On the other hand, let the auxiliary signals $w_\Delta$, $z_\Delta$ be related by the equation $w_\Delta = \Delta z_\Delta$ where

$$\Delta = diag(\delta_{p1}, \delta_{p2}, \delta_{p3}, \delta_{z1}, \delta_{z2}, \delta_{z3}).$$

Minimizing the $H_\infty$ norm of the transfer function $T_{z_\Delta w_\Delta}$ would increase the robust stability margin of the modulator.

In the following we invoke the $H_\infty$ control theory to accomplish the control strategies discussed earlier. To this end, the proposed compensated ΣΔ modulator architecture (see Fig. 3) is converted to the general framework in Fig. 2, where x=[$x_1$ $x_2$ $x_3$ $x_{IM}$ $x_{Q_1}$ $x_{Q_2}$ $x_W$]$^T$ (represents a collection of the states of $H_1$, $H_2$, $H_3$, $K_{IM}$, $Q_1$, $Q_2$ and $W$), $z=[z_\Delta^T \; e \; \tilde{u}_1]^T$, $w=[w_\Delta^T \; R \; E_1 \; E_2]^T$, $u = Y$, $y=y_{IM}$, $K=K_1$.

Accordingly, the robust digital filter design problem is formulated as the following $H_\infty$ control problem:

$$\min_{K_1} \|T_{zw}\|_\infty \tag{8}$$

By the small gain theorem, if $K_1$ is determined such that the closed-loop system is stable and its H-infinity norm is less than $\gamma$, then it is guaranteed that the closed-loop system is stable against the uncertainties $\Delta$ with sizes no greater than $1/\gamma$. The problem can be efficiently solved by the MATLAB command dhinflmi [14]. The resulting filter is given by $F = K_1 K_{IM}$.

## IV. Simulations

The proposed MASH 2-1 architecture has been simulated in MATLAB/SIMULINK environment [14,15]. The modulator is designed in accordance with the proposed scheme in Section III. From a practical aspect, the modulator of this experiment is aimed at applying to an audio system. The simulation parameters used are summarized in Table 1. $Q_1$ and $Q_2$ are calculated by (3). Moreover, the weighting function $W$ is chosen to be $(80z^{-1})/(1+0.775z^{-1})$.

By using the Matlab function "dhinflmi" to solve problem (8), it yields the digital filter $F = K_1 K_{IM}$ where

$$K_1 = 10^7 \times \frac{0.0682z^{-1} - 0.3697z^{-2} + 0.9432z^{-3} - 1.4805z^{-4} \cdots}{1 - 3.0559z^{-1} + 3.8943z^{-2} - 2.6470z^{-3} + 1.0226z^{-4} \cdots}$$
$$\frac{+1.5464z^{-5} - 1.0818z^{-6} + 04858z^{-7} - 0.1256z^{-8} + 0.0141z^{-9}}{-0.2407z^{-5} + 0.0595z^{-6} - 0.0431z^{-7} + 0.0147z^{-8} + 4.2821\times 10^{-17} z^{-9}}$$

and the closed-loop poles are (-0.0003, $5.9119\times10^{-10}$, 0.021456, $0.95589 \pm 0.053916i$, 0.83713, $0.38486 \pm 0.13382i$, 0.53705, $0.48952 \pm 0.018995i$, 0.50001, $0.75 \pm 0.43301i$, $0.75 \pm 0.43301i$, 0.5) which are all within the stability region, i.e., the open unit disk. The $H_\infty$ norm of $T_{zw}$ reads 361.6409 which in turn guarantees a conservative lower bound of the robust stability margin as 0.0028; that is, the compensated modulator remains stable at least for the range of deviations $\delta_{z_i} \in [0, 0.0028)$ and $\delta_{p_i} \in [0, 0.0028)$ in the values of $\beta_i$ and $\alpha_i$ of the integrators (see (7)), corresponding to insufficient op amplifier gain and capacitor ratio mismatch [16]. In the following, the imperfections associated with the integrator gains and the poles are assumed to be $\delta_{p_i} = \delta_{z_i} = 0.001$.

TABLE 1: Simulation parameters

| Parameter | Value |
|---|---|
| Signal bandwidth | 25 kHz |
| over-sampling frequency ($F_S = 1/T_S$) | 12.8MHz |
| over-sampling ratio | 256 |
| Input signal frequency | 6.25kHz |
| Input signal amplitude range | -140 dB to 60 dB |
| Samples number | 65536 |
| Swing limit | +1/-1 |
| Path coefficients | $a_1$=0.5; $a_2$=0.5; $b_1$=0.5; $b_2$=0.5; $b_3$=0.5; |

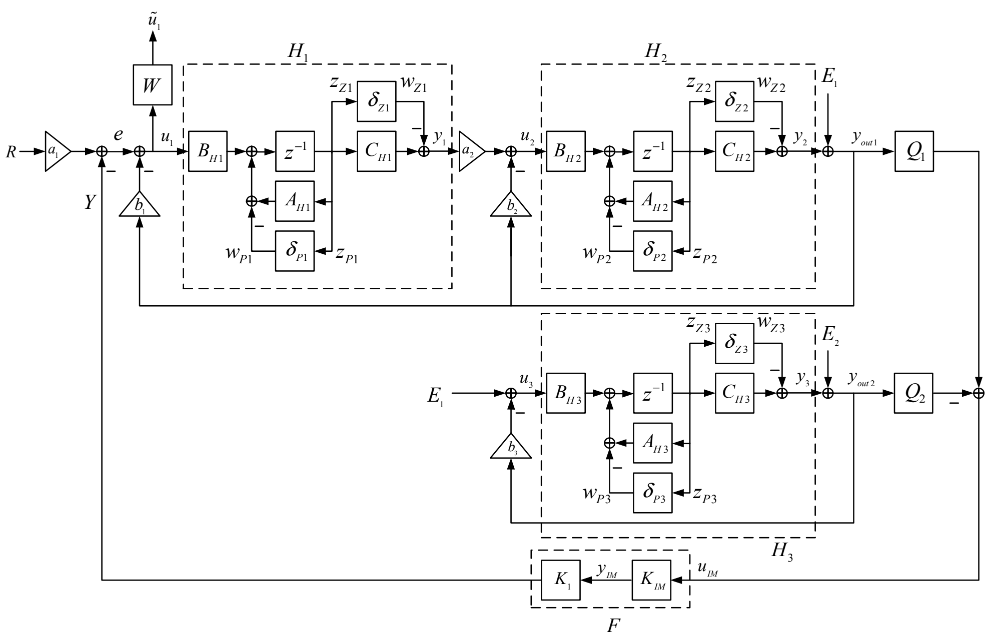


Figure 3. Proposed MASH 2-1 modulator

Fig. 4 shows SNR performance vs. input amplitude for the proposed ΣΔ modulator and the conventional one. It is known that the maximum input signal level that the modulator can handle and the minimum detectable input signal is the so-called "dynamic range". As can be seen the proposed robust ΣΔ modulator not only has a much better peak SNR performance, but also its DR is significantly increased by the proposed digital compensation technique. More precisely, the peak SNR performance obtained by the proposed ΣΔ modulator occurs in 148.9 dB (an effective resolution of 24 bits calculated by (6)) while the input level is 39.5 dB. Compared with the conventional ΣΔ modulator, the improvement is 65.81 %, from 89.8 dB to 148.9 dB. As for the SNR performance, it is noted that the proposed robust ΣΔ modulator performs slightly better than the conventional one when the input amplitude is less than -19.9dB. As the input level increases further, while the SNR value of the proposed ΣΔ modulator keeps growing, that of the conventional ΣΔ modulator falls down dramatically. This observation motivates us to take the advantages of the interesting property of the proposed modulator to further improve its SNR performance. The idea comes up to redesign the H-infinity-control-based modulator by increasing the value of the path coefficient $a_1$ by a factor $\sigma$. Equivalently, this leads to a shift of the SNR curve of the proposed modulator in Fig. 4 to the left by an amount of $20 \log \sigma$ dB. For a full coverage of the operating range for the input (Here it is defined as the range less than 1 volt, i.e., 0 dB), it is, however, not appropriate to apply the same skill to the conventional ΣΔ modulator. The result of the redesign with $\sigma = 100$ is shown in Fig. 5, compared with the conventional modulator. Obviously, the SNR performance of the proposed modulator has been greatly improved. At the same time, it is interesting to note that the DR remains unchanged because the nature of the curve shifting.

Table 2 shows the output of the integrators for both of the modulators with 1 volt, i.e. 0dB, input. It is shown that the output swings of the proposed modulator are correspondingly lower than those of the conventional one. In fact, signal clipping occurs at the first integrator of the conventional modulator, and causes saturation (the saturation level is +1/-1), which in turn degrades the SNR performance as shown in Fig.4.

In Fig. 6, one can see clearly that the harmonics resulting from signal clipping appear on the output spectrums of the modulators. Finally, the simulation results of SNR versus input amplitude are reproduced in Fig. 7 for the various kinds of imperfections associated with integrator gains and poles. It is shown that the proposed modulator indeed exhibits high SNR performance at large inputs. In addition, it is also validated by simulation that the tracking error $e$ due to step or ramp type input $R$ is small, which confirms the efficacy of the proposed design.

TABLE 2: output swing of the integrators

| Integrator | architecture | Output swing |
|---|---|---|
| Integrator $H_1$ | conventional | 0.9990~-0.9990 |
| | proposed | 0.8831~-0.8923 |
| Integrator $H_2$ | conventional | 0.9630~-0.9627 |
| | proposed | 0.7052~-0.7067 |
| Integrator $H_3$ | conventional | 0.9990~-0.9990 |
| | proposed | 0.9990~-0.9990 |

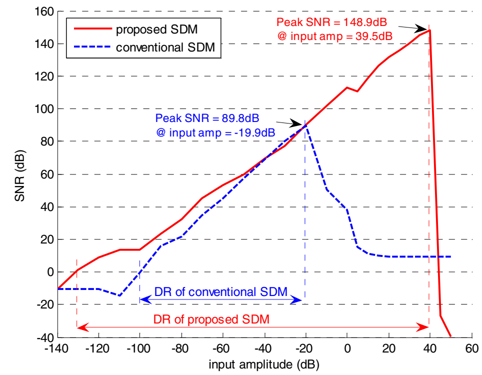


Figure 4. Comparisons of the SNR value and the dynamic range associated with the conventional and the proposed robust ΣΔ modulators

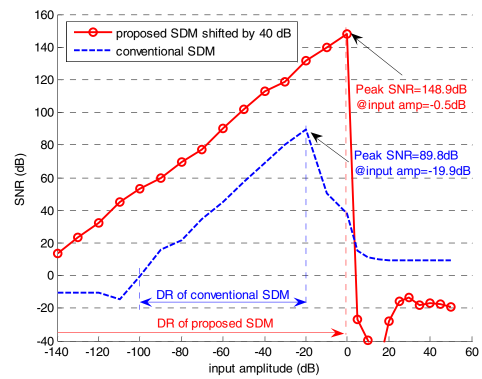


Figure 5. Comparisons of the SNR value and the dynamic range associated with the conventional and the redesigned robust ΣΔ modulators

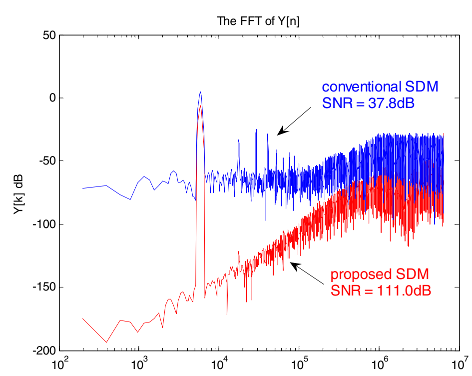


Figure 6. Power spectrum density associated with the conventional and the proposed robust ΣΔ modulators

the proposed approach to the other architecture for low and middle frequencies applications is straightforward.

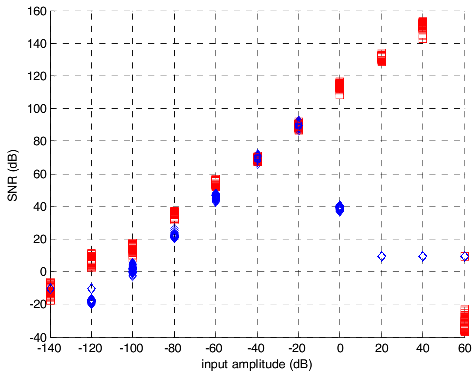


Figure 7. Parameters imperfections $\delta_{p_i}$ , $\delta_{z_i}$ deviate from 0.0001 to 0.002. Diamonds –conventional filter results; Squares –robust filter results.

## V. CONCLUSIONS

A new digital compensation scheme for MASH sigma-delta modulator with analog imperfections has been presented. Specifically, The SNR performance enhancement problem and the output swing suppression problem were formulated, from the viewpoint of control, as a robust tracking control problem. Internal model principle and H-infinity control theory were invoked to design the robust digital filter for a MASH sigma-delta modulator with 2-1 structure. Numerical experiments show that the proposed modulator exhibits superior capability for handling large inputs, which in turn leads to a much wilder dynamic range than the conventional one, though the SNR performance for the both are about the same for the input less than -20dB. Accordingly, a simple redesign, benefited from the wide dynamic range, was presented, which greatly improved the SNR performance. An effective resolution of 24 bits is obtained for the proposed modulator. Output swing suppression was validated by the numerical results. The limitations of the proposed design for higher frequencies applications and hardware implementation are under investigation. Extension of

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