The Improvement of Conditional Sum Adder for Low Power Applications

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Abstract

This work describes a new conditional-sum addition rule for low power applications. This conditional sum adder is especially attractive for implementing high-speed arithmetic systems. The new conditional sum addition rule can reduce the internal nodes and multiplexer numbers of the adder design. Various supply voltages and circuit structures are used to implement the new conditional sum adders. It's shown that about 10% to 25% power-delay product is saved.

I. Introduction

In recent years, power dissipation is becoming an important constraint not only is portable electronic systems but also for high integrated density. The increasing demand for high-speed battery-powered digital signal processing systems has increased the demand for high-speed low-power digital circuits and digital subsystems. The increased amount of data for high performance DSP system requires more efficient methods for processing the data as well as building faster architectures and low power dissipation to handle the data processing in real-time.

Addition is the basic operation of the digital signal processing. It is shown that the conditional sum adder has a better power-delay product than other adders for high-speed applications [1], [7]. In this work a new conditional sum addition rule called the conditional carry addition rule is proposed. The improvement of the conditional sum adder can reduce the internal nodes and multiplexer numbers of the adder design. Thus the new conditional carry adders have less parasitic capacitive load and hence have less power dissipation. The static CMOS logic circuit [6] and the CPL circuit [2], [5] are used to design the proposed new adder structures. The simulated supply voltage is changed from 3.3V to 1.2V.

II. Adder Structure

A. Ripple Carry Addition Rules

The speed of digital arithmetic processor depends on the speed of the adders used in the system. As shown in Fig. 1, the ripple carry addition rule has the simplest adder structure. The shadow block is a one-bit addition. The arrows show the actual carriers generated and propagated between one-bit adders. It is clear that the total propagation delay of an n-bit ripple carry adder is linearly proportional to the length n of the adder. It has large delay time for large n. As shown in Fig. 4, the carry lookahead adder (CLA) can implement 4-bit addition in a 4-bit CLA unit. Thus the carry ripple length of a **n**-bit adder is reduced to **n**/4 of 4-bit CLA units.

B. Conditional Sum Addition Rules

As shown in Fig. 2, the conditional sum addition rules can overcome the carry propagation problem [3], [9]. It generates distant carriers and using these carriers to select the true sum outputs from two simultaneously generated provisional sums under different carry input conditions. Fig. 2 shows the 8-bit addition, where the arrows show the actual carries generated between sections. It is seen that simultaneous additions are performed on all section independently. The addition process of a n-bit adder is completed in t steps, where

$$t = \lceil \log_2 n \rceil. \qquad (1)$$

C. Condition Carry Addition Rule

An improvement of the conditional-sum addition rule called the condition carry addition rules is shown in Fig. 3. It also has no carry propagation problem. The generated distant carriers are used to select the true carry outputs from two simultaneously generated provisional carrier under different carry input conditions. The arrows show the actual carriers generated between sections. The simultaneous carry generations are performed on all section independently. The conditional carry addition of an 8-bit adder is completed in 3 steps. An extra XOR function of the C_{out} and S^0 is required to generate the final sum outputs,

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the final addition results.

D. Adder Structure

The 8-bit conditional sum adder and the proposed 8-bit conditional carry adder are shown in Fig. 6 and Fig. 7, respectively. Fig. 7(a) is the condition carry adder structure. The carry outputs C_i are generated by conditional carry unit. The XOR gates are used to execute the final addition outputs. As shown in Fig. 7(b), the conditional carry unit is implemented by 2-input MUX.

It is clear that the conditional carry unit processing fewer signals than the conditional sum adder during the three conditional carry select steps. Thus it can reduce the internal nodes and MUX numbers of the adder design and cause to reduce internal parasitic capacitive load. Thus the hardware, operation speed and power dissipation are improved. Table 1 shows the number of 2-input MUX gate used to implement the n-bit conditional sum adder (CSA) and the proposed n-bit conditional carry adder (CCA).

	Num. of MUX gates	
n-bit adder	CSA	CCA
8	28	17
16	75	49
32	186	129
64	441	321
128	1016	769

Table 1. The multiplexer numbers comparison.

E. Circuit Implementation

The static CMOS circuit and the CPL circuit [2], are used to implement the n-bit conditional sum adder and conditional carry adder. The circuit schematic of the CPL as shown in Fig. 5, is taken to be the trend on low-power digital design because of the half capacitance thus saving 1/2 transient power than other than conventional CMOS digital circuits. Conventionally, CPL utilizes a PMOS cross-coupled latch to regenerate signal form CPL logic tree and two static inverters are used to drive next stages. The Carry lookahead adders implemented by the static CMOS circuit are also given.

III. Simulation Results

The HSPICE simulations are based upon 0.5 um CMOS technology where the threshold voltages of the NMOS and PMOS transistors are 0.74V and –0.92V, respectively. The simulated average delay, power dissipation, and power-delay production of the 16-bit and 32-bit adders using the static CMOS logic circuit and the CPL circuit are shown in Table 2 to Table 7. The simulated supply voltages are various from 1.2V to 3.3V.

It is seen from the simulation results, that the proposed new conditional carry adders (CCA) have better power-delay performance than the conditional sum adders (CSA) and the carry lookahead adders (CLA). For high supply voltage (3.3V) applications, the static CMOS circuit shows the performance advantage than the CPL logic circuit. For low voltage (less than 2.0V) applications, the CPL circuits have better circuit performance. It also find that the CLA adder structure has fewer power dissipation than the others. But it has long critical delay.

IV. Conclusion

In this work, an improved conditional sum addition rule is used to design the new conditional carry adder for high speed and low power applications. Various supply voltages and circuit structures are used to implement the new conditional carry adder. The HSPICE simulation results show that about 10% to 25% of power-delay product is saved of this new adder. The comparison and optimization of different logic circuits for various supply voltages are also shown for low power and high-speed applications.

References

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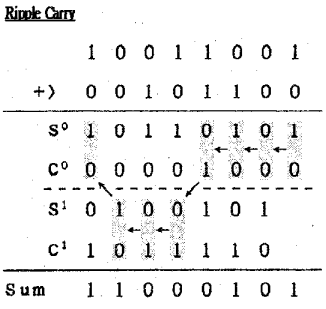


Fig.1. Ripple carry addition rule.

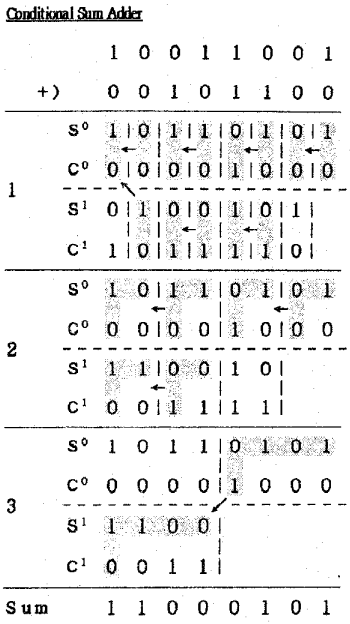


Fig. 2. Conditional sum addition rule.

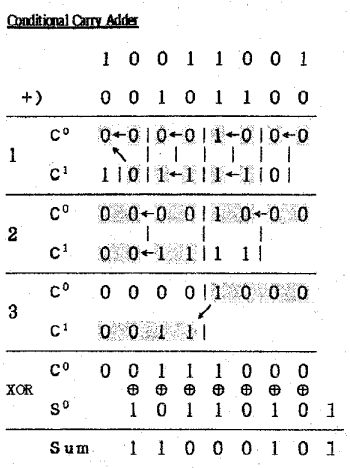


Fig. 3. Conditional carry addition rule.

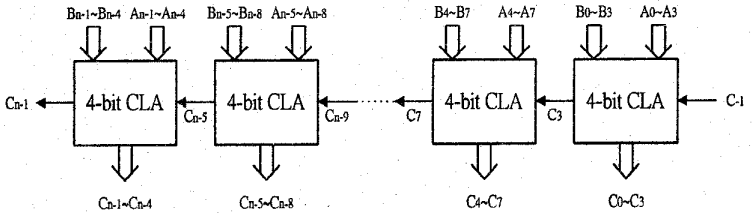


Fig. 4. Carry Lookahead Adder.

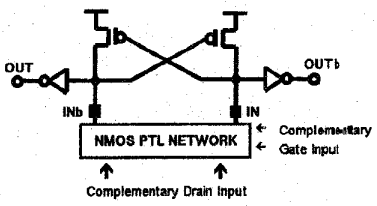


Fig. 5. The CPL Circuit Diagram.

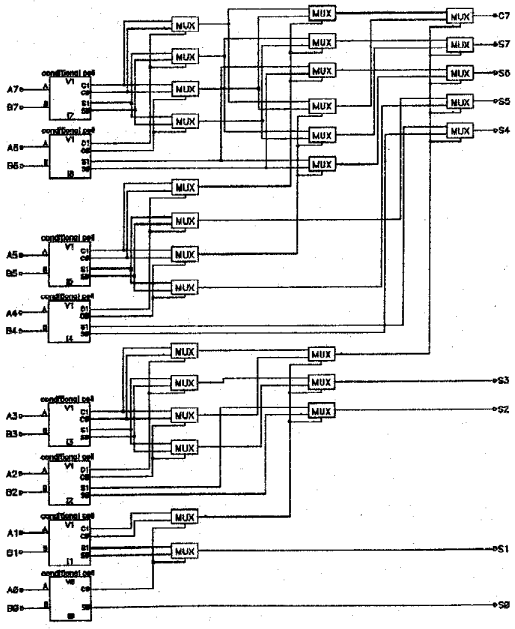
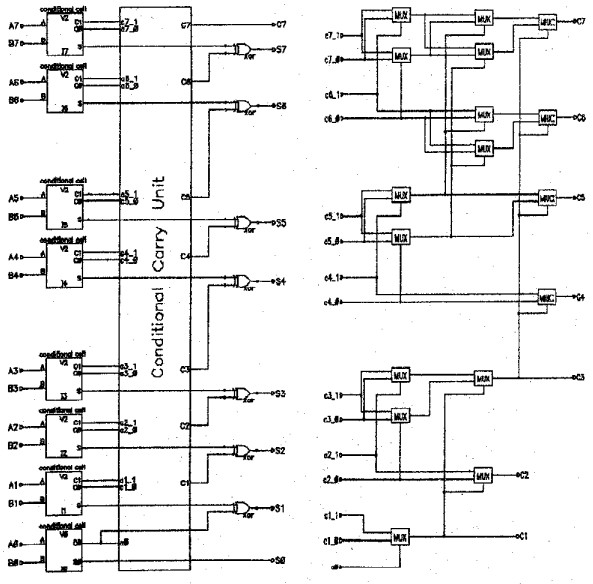


Fig. 6. Conditional Sum Adder.



(a) Conditional Carry Adder. (b) Conditional Carry Unit.

Fig. 7.

Average delay of 16-bit adder unit:n sec

supply	new (CCA)		old(CSA)		CLA
voltage	static	cpl	static	cpl	static
1.2		33.59		30.76	
1.3		22.57		20.94	61.09
1.4	22.47	16.80		15.77	45.93
1.5	16.47	13.36	15.81	12.72	36.16
1.6	11.61	11.11	12.68	10.67	29.66
1.7	8.88	9.51	10.54	9.18	25.00
1.8	7.31	8.30	9.00	8.12	21.58
1.9	6.20	7.38	7.87	7.30	19.05
2.0	5.39	6.63	6.98	6.65	17.04
2.1	4.80	6.05	6.27	6.14	15.42
2.2	4.33	5.55	5.70	5.68	14.13
2.3	3.96	5.13	5.21	5.31	13.05
2.4	3.65	4.65	4.80	4.97	12.06
2.5	3.38	4.45	4.47	4.69	11.25
2.6	3.16	4.18	4.18	4.44	10.58
2.7	2.97	3.96	3.91	4.21	9.97
2.8	2.79	3.75	3.68	4.02	9.44
2.9	2.64	3.57	3.34	3.85	8.97
3.0	2.50	3.39	3.31	3.68	8.55
3.1	2.38	3.26	3.16	3.53	8.17
3.2	2.29	3.12	3.03	3.41	7.85
3.3	2.18	2.99	2.90	3.29	7.55

Table 2.

Average delay of 32-bit adder unit:n sec

supply	new (CCA)		old (CSA)		CLA
voltage	static	cpl	static	cpl	static
1.2		41.35		38.34	
1.3		27.76		25.95	
1.4	23.88	20.65		19.48	
1.5	19.60	16.43	20.33	15.62	67.89
1.6	13.71	13.68	16.44	13.10	56.76
1.7	10.94	11.70	13.70	11.26	48.00
1.8	8.79	10.24	11.74	9.92	41.48
1.9	7.58	9.09	10.24	8.88	36.50
2.0	6.69	8.17	9.07	8.08	32.69
2.1	5.99	7.45	8.17	7.41	29.52
2.2	5.42	6.86	7.41	6.88	27.05
2.3	4.96	6.33	6.77	6.39	24.96
2.4	4.57	5.87	6.05	5.98	23.16
2.5	4.23	5.50	5.56	5.67	21.59
2.6	3.95	5.16	5.18	5.36	20.22
2.7	3.71	4.88	4.85	5.09	19.07
2.8	3.49	4.62	4.39	4.88	18.05
2.9	3.30	4.40	4.12	4.67	17.17
3.0	3.13	4.19	3.92	4.48	16.34
3.1	2.98	4.01	2.72	4.33	15.65
3.2	2.85	3.85	3.55	4.18	15.01
3.3	2.73	3.70	3.38	4.05	14.42

Table 3.

rms power of 16-bit adder unit: mW

supply	new (CCA)		old (CSA)		CLA
voltage	static	cpl	static	cpl	static
1.2		0.59		0.62	
1.3		0.79		0.82	0.15
1.4	1.34	0.98		1.02	0.18
1.5	1.60	1.20	1.63	1.26	0.21
1.6	1.91	1.47	1.93	1.54	0.25
1.7	2.25	1.78	2.28	1.87	0.29
1.8	2.62	2.08	2.67	2.20	0.35
1.9	3.03	2.47	3.09	2.62	0.40
2.0	3.47	2.86	3.53	3.03	0.45
2.1	3.97	3.31	4.04	3.52	0.51
2.2	4.48	3.75	4.56	3.99	0.58
2.3	4.99	4.24	5.08	4.52	0.67
2.4	5.56	4.79	5.66	5.12	0.76
2.5	6.13	5.4	6.25	5.77	0.86
2.6	6.82	6.02	6.94	6.43	0.96
2.7	7.49	6.66	7.63	7.11	1.08
2.8	8.22	7.34	8.36	7.87	1.20
2.9	8.97	8.09	9.11	8.69	1.32
3.0	9.76	8.89	9.92	9.56	1.46
3.1	10.61	9.76	10.77	10.49	1.61
3.2	11.51	10.64	11.67	11.43	1.76
3.3	12.36	11.49	12.53	12.40	1.93

Table 4.

rms power of 32-bit adder unit: mW

supply	new (CCA)		old (CSA)		CLA
voltage	static	cpl	static	cpl	static
1.2		1.23		1.28	
1.3		1.66		1.70	
1.4	2.73	2.08		2.16	
1.5	3.27	2.54	3.34	2.67	0.42
1.6	3.95	3.08	4.02	3.24	0.48
1.7	4.57	3.73	4.66	3.92	0.54
1.8	5.33	4.38	5.46	4.63	0.62
1.9	6.17	5.20	6.32	5.50	0.69
2.0	7.06	6.02	7.24	6.37	0.77
2.1	8.07	6.99	8.28	7.41	0.85
2.2	9.11	7.93	9.35	8.42	0.95
2.3	10.16	8.96	10.44	9.53	1.08
2.4	11.32	10.15	11.63	10.81	1.20
2.5	12.50	11.46	12.87	12.21	1.34
2.6	13.91	12.78	14.31	13.62	1.47
2.7	15.28	14.17	15.71	15.09	1.62
2.8	16.77	15.64	17.23	16.72	1.78
2.9	18.31	17.27	18.81	18.48	1.94
3.0	19.94	19.00	20.49	20.35	2.10
3.1	21.70	20.88	22.26	22.35	2.26
3.2	23.55	22.80	24.14	24.37	2.45
3.3	25.31	24.67	25.94	26.48	2.67

Table 5.

power-delay product of 16-bit adder unit: p J

supply	new (CCA)		old (CSA)		CLA
voltage	static	cpl	static	cpl	static
1.2		19.89		18.97	
1.3		17.83		17.25	8.85
1.4	30.16	16.44		16.11	8.18
1.5	26.35	**15.98**	25.73	**16.01**	7.59
1.6	22.18	16.43	24.52	16.51	**7.28**
1.7	19.96	16.92	**23.98**	17.19	7.36
1.8	19.17	17.29	24.02	17.90	7.52
1.9	18.79	18.23	24.30	19.11	7.66
2.0	**18.68**	18.95	24.67	20.15	7.67
2.1	19.06	20.04	25.31	21.60	7.84
2.2	19.38	20.84	26.00	22.68	8.26
2.3	19.74	21.74	26.45	23.97	8.71
2.4	20.27	22.78	27.12	25.42	9.14
2.5	20.74	24.07	27.92	27.07	9.61
2.6	21.55	25.16	29.03	28.52	10.19
2.7	22.22	26.36	29.81	29.96	10.72
2.8	22.92	27.47	30.78	31.67	11.30
2.9	23.70	28.82	31.83	33.45	11.87
3.0	24.40	30.16	32.81	35.22	12.49
3.1	25.27	31.77	34.04	37.08	13.13
3.2	26.31	33.19	35.38	39.00	13.83
3.3	26.97	34.37	36.37	40.81	14.53

Table 6.

power-delay product of 32-bit adder unit: p J

supply	new (CCA)		old (CSA)		CLA
voltage	static	cpl	static	cpl	static
1.2		50.66		49.01	
1.3		46.12		44.13	
1.4	65.12	42.89		42.15	
1.5	64.13	**41.71**	67.88	**41.64**	28.51
1.6	54.09	42.16	65.99	42.45	27.24
1.7	49.96	43.58	**63.84**	44.15	25.92
1.8	46.80	44.78	64.13	45.90	25.72
1.9	**46.76**	47.24	64.74	48.85	25.19
2.0	47.20	49.18	65.66	51.48	25.17
2.1	48.34	52.04	67.64	54.92	**25.09**
2.2	49.35	54.36	69.32	57.87	25.70
2.3	50.37	56.73	70.67	60.90	26.69
2.4	51.75	59.58	70.39	64.65	27.79
2.5	52.87	63.05	71.75	69.18	28.93
2.6	55.01	66.02	74.10	73.01	29.72
2.7	56.66	69.12	76.20	76.71	30.89
2.8	58.44	72.26	75.58	81.23	32.13
2.9	60.38	75.92	77.55	86.27	33.31
3.0	62.42	79.62	80.31	91.17	34.31
3.1	64.61	83.80	82.68	96.66	35.37
3.2	67.12	87.71	85.60	101.80	36.77
3.3	68.96	91.20	87.56	107.20	38.50

Table 7.