Implement An All In One 315MHz ASK UHF Receiver

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ABSTRACT–**An all in one integrated 315MHz ASK UHF receiver is proposed in this paper. This receiver has several characteristics, first RF-in data-out all in one function, second without any spiral inductor and final filter all on chip [1][2]. We design a monolithic ultra-high frequency (UHF) receiver including RF front-end, intermediate-frequency (IF) stage and base-band stage. The RF front-end end include single end low-noise amplifier (LNA) without on-chip spiral inductors and a mixer which down-converters the LNA output to 2.25MHz IF. The IF stage includes 1MHz Band pass filter, variable-gain amplifier (VGA), automatic gain control (AGC) loop and peak detector. The base-band stage includes on-off keying (OOK) demodulator and slicing comparator to output digital signal. The UHF receiver was implemented in a UMC 0.5μm CMOS process. The receiver sensitivity is -73dBm and 2.4kbits data rate. The chip consumes 13mA and size in 1370x1370μm2. In the future, we will increate the sensitivity to –100dbm, then this receiver will be manufactured into product. Thus the design of a high sensitivity and low cost UHF receiver will be the most important area for the future work.**

Keywords–**UHF receiver, ASK receiver.**

1. INTRODUCTION

Wireless communication has developed dramatically in recent years such as wireless (cordless and cellular) phone, global positioning system (GPS) and wireless local area network (LNA). Although many researches have devoted to high-frequency wireless receiver, ultra-high-frequency (UHF) wireless receiver still plays a significant role to implement the wireless communication to our daily lives. The applications of ultra-high-frequency wireless receivers such as remote keyless entry, security system, remote control system, long-rang RF ID and car alarm system are growing rapidly and need to be more concern about it.

Fig1.1 is a typical wireless receiver [3]. The whole receiver is usually partitioned to three partitions: RF, IF and baseband. RF/IF function includes three major function : signal amplification and filtration, frequency translation and frequency generation. The LNA amplifies the received signal, which is then passed through a band-select filter, which filters out the out-of-band noise and selects the band signals we want. The mixer and RF synthesizer perform the frequency translation of the signals, the bandpass filter performs channel-select of the signal we want. Finally, signals are demodulated by a demodulator and formed the digital data output.

In order to meet the stringent requirements in wireless system, many external components like bandpass filter in IF, lowpass filter in baseband and stable crystal oscillator are generally employed in the conventional wireless receiver. Due to the convenience and commercial considerations, the demands of low-cost specification, the area of the receiver and the number of discrete components must be reduced. It also means that a monolithic receiver integrated circuit will be more popular. Therefore, utilizing the integrated circuits to implement the external components becomes an import research aspect to the design of UHF receiver.

We propose the architecture of UHF receiver shown in Fig.1.2. The functions of receiver are completely integrated and make the receiver a highly reliable low cost solution for high volume wireless communications. The receiver consists of a low-noise amplifier, a downconversion mixer, an automatic gain control (AGC) loop, an OKK demodulator, a frequency-tuning circuit and bandgap.

2. CIRCUIT DESIGN

2.1 Low Noise Amplifier Design

Four different architectures that can be employed for LNA are shown in g.2.1 [4][5]. Four different architectures that can be feedback amplifier are shown in Fig.2.2. In the Chip, we don't need use spiral inductor LNA. We use the feedback system architecture for our LNA in Fig. 2.2(c)[6]. The LNA architecture includes low noise amplifier circuit, bias circuit, frequency tuning circuit and DC level feedback

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circuit in Fig.2.3. The DC level feedback circuit extracts DC level from LNA output and feedback to stable the circuit operation. The simulate result in Fig.2.4 to Fig.2.9.

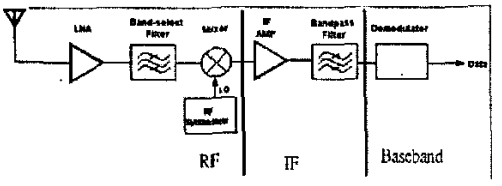

Fig 1.1. Typical wireless receiver architecture

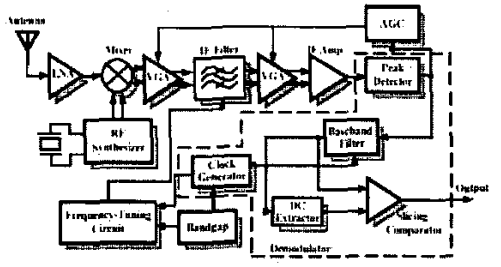

Fig. 1.2. The proposed UHF ASK receiver

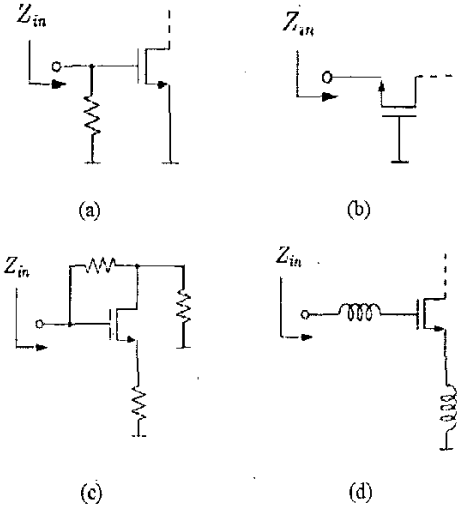

Fig.2.1. Four different LNA architectures for impedance matching topologies: (a) resistive termination topology. (b) 1/gm termination topology. (c) Resistive shunt-series feedback topology. (d) Inductive degeneration topology.

2.2 Mixer Design

Mixers perform frequency translation by multiplying two signals (and possibly their harmonics). Downconversion mixer employed in the receive path have two distinctly different inputs, called the RF port and the LO port. The RF port senses the signal to be downconverted and LO port senses the periodic wave generated by the local oscillator. Then output 2.25MHz signal to IF. If a mixer accommodates a differential LO single-ended RF signal, it is called "single balanced," an example being the topology shown in Fig.2.10 (a). If a mixer operates with both differentials LO and RF inputs, then it is called "double balanced," the active version of which assumes the form of a Gilbert cell in Fig.2.10 (b). The double-balanced mixer generates less even-order distortion, thus relaxing the half-IF issue in heterodyne receivers and lowering the beat components in homodyne architectures. So, we use this architecture.

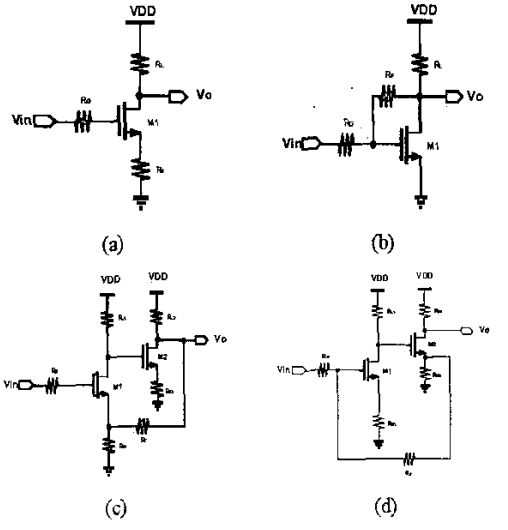

Fig.2.2. The four basic feedback topologies: (a) current-sampling series-mixing topology.(series- series feedback amplifier) (b) voltage-sampling shunt-mixing topology. (shunt-shunt feedback amplifier) (c) voltage-sampling series-mixing topology. (series-shunt feedback amplifier) (d) current-sampling shunt-mixing topology.(shunt- series feedback amplifier)

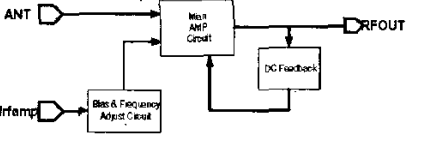

Fig.2.3. The LNA architecture

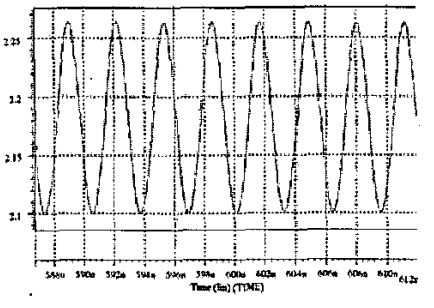

Fig.2.4. Output waveform of LNA. Vp-p=165mV.

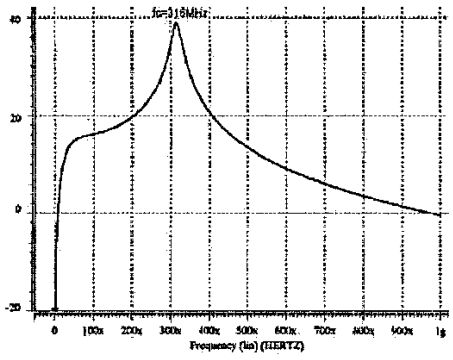

Fig.2.5. Frequency response of LNA. The maximum gain is 38.9dB at 316MHz.

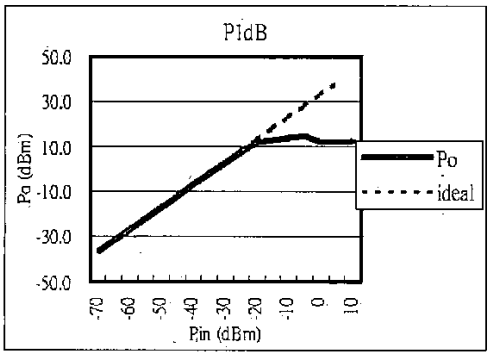

Fig.2.6. P1dB compression point of LNA.

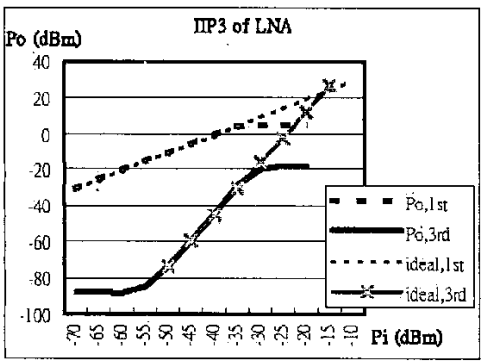

Fig.2.7. IIP3 compression point of LNA.

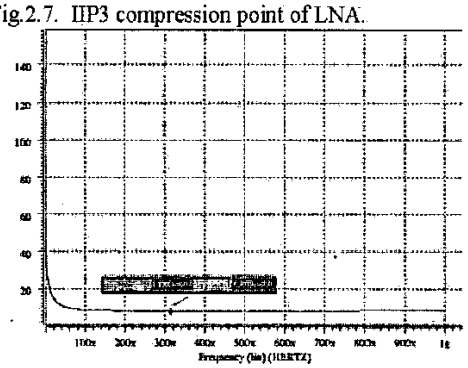

Fig.2.8. Noise figure of LNA. The noise figure is 7.97dbm at 315MHz.

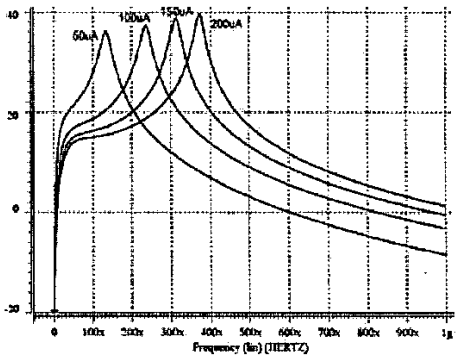

Fig.2.9. The waveform of Irfamp.

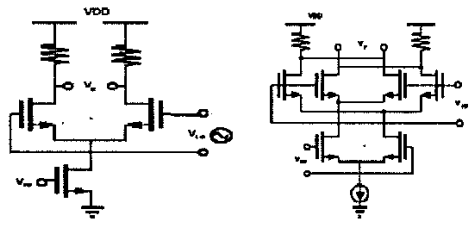

Fig.2.10. (a) Single-balanced mixer, (b) double-balanced mixer.

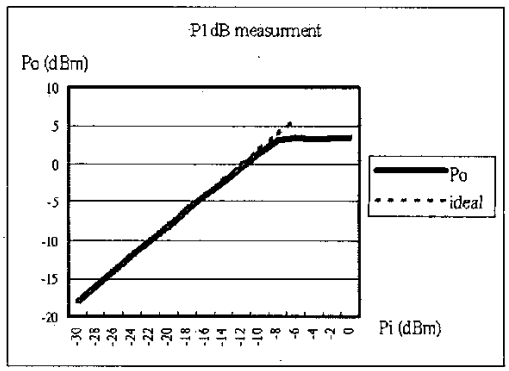

Fig.2.11. P1dB of mixer

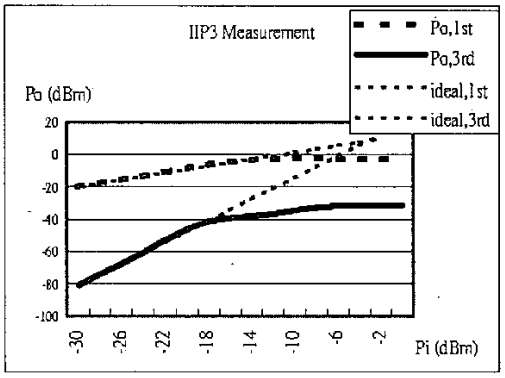

Fig.2.12. IIP3 of mixer

2.3 *IF Stage*

The block diagrams of IF stage are shown in Fig.2.13 [7][8]. The IF stage consists: variable gain amplifier (VGA), IF bandpass filter, IF amplifier, peak detector and automatic gain control (AGC)[9][10][11]. The feedback loop comprises VGA, IF amplifier, peak detector and AGC connected together also called an AGC loop. The AGC loop in the proposed UHF receiver is in order to keep the magnitude of the output signal constant despite the large dynamic range of the input amplitude. The simulation result of IF stage are shown in Fig.2.14. The simulation of UHF receiver is shown in Fig.2.15.

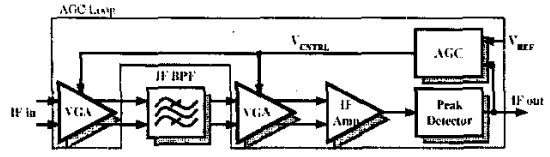

Fig.2.13. The IF system block

3. MEASUREMENT RESULTS

Fig.2.16 shows the receiver chip how to implement for measurement. We use signal generator force ASK signal to antenna (ANT pin) and use scope measurement the data from Do pin. The measurement result is shown in Fig.2.17. Fig.2.18 shows the transmitter and receiver how to implement for measurement. We use signal generator force data to transmitter. Then, transmitter transmit ASK signal from antenna and receiver receive ASK signal from antenna. The measurement result is shown in Fig.2.19.

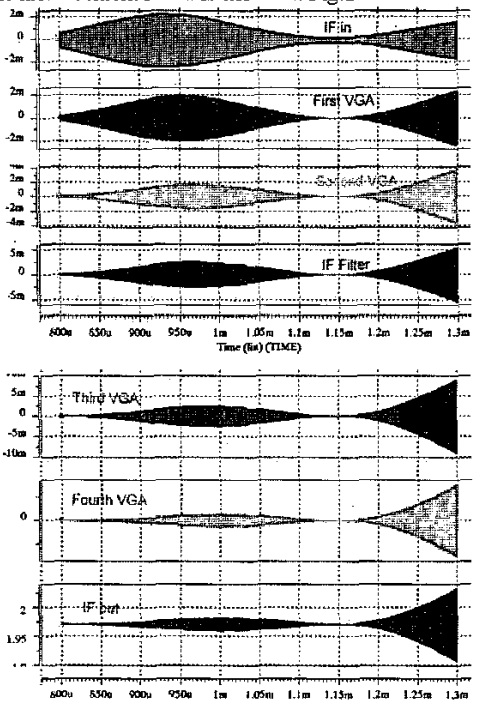

Fig.2.14. The result of IF circuit simulation.

4. CONCLUSIONS

In this paper, the simulation results of whole UHF receiver system are also shown. The individual simulated result of front-end stage, IF stage and receiver system are presented, respectively. The front-end stage presents the amplification and the frequency transition of the RF signal. The function of the IF stage is to amplify the input signal of IF stage and maintain the magnitude of the output signal of IF stage not to saturate the subsequent stage. The simulation results of the receiver system show that the receiver is a "RF in, data out" system and exhibits integrated filter and automatic gain control [12][13][14][15]. Final, The receiver is implemented and shown the result in Table 1.

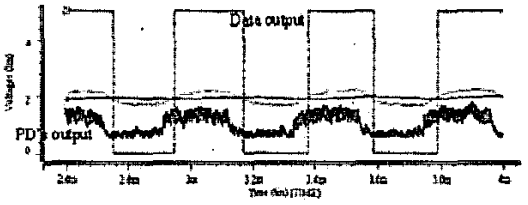

Fig.2.15. The Digital output of UHF receiver.

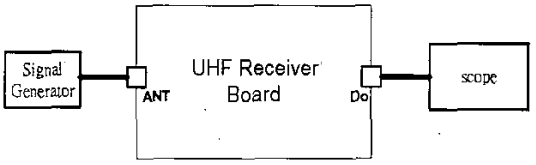

Fig.2.16. Configuration of UHF receiver for measurement

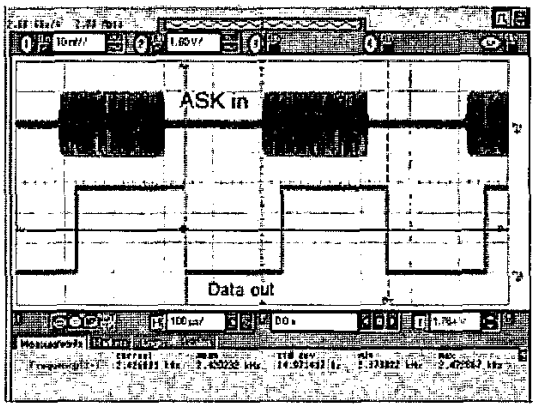

Fig.2.17. Measurement result of UHF receiver chip

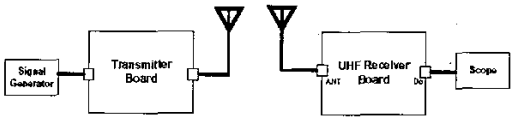

Fig.2.18. Configuration of RF system for measurement

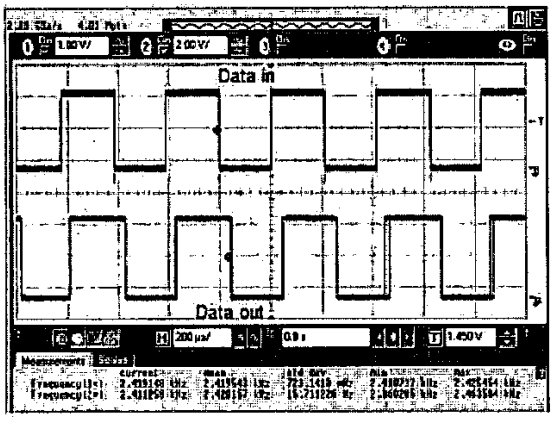

Fig.2.19. Measurement of RF system

Table 1. Summary of UHF receiver chip performance

Parameter	SPEC.	Unit
Power supply	5	voltage
Modulation	ASK	
Data rate	1~7.8	MHz
Receiver sensitivity	-10~-73	dBm
Ant freq. (RF)	315	MHz
Local freq. (LO)	312.75	MHz

ACKNOWLEDGMENTS

The authors would like to thank the National Science Council, Taipei, China for the financial support under Contracts NSC 92-2213-E-032-003 and NSC 92-2215-E-002-019/009, and the funding from Tamkang University to support the Department of Electrical Engineering.

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