# CGIN: A Modified Gamma Interconnection Network with Multiple Disjoint Paths ${ }^{1}$ 

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#### Abstract

To ensure high terminal reliability for the Gamma interconnection network (GIN), we propose a new modified GIN, referred to as CGIN as its connecting patterns between stages exhibit a cyclic feature. The fact that there exist multiple disjoint paths between any communication pair for all types of CGINs makes it possible to tolerate any arbitrary single fault and to accomplish enhanced terminal reliability accordingly. The performance of the CGIN is also evaluated through simulation.


## 1. Introduction

With the advance of VLSI technology, research on multiprocessors is drawing more and more attention. In the development of multiprocessors, the design of its interconnection networks plays quite an important role since it governs the performance of the whole system. The multistage interconnection network (MIN), to give an example, stands as one very significant production of such networks. It is employed in a multiprocessor to connect processors and memory modules together, using multiple stages of small crossbar switches of a fixed size. The Omega network [1], Binary n-cube network [2], and Baseline network [3] are all MINs composed of $2 \times 2$ switches. However, they provide only a unique path between any source-destination pair, unable to tolerate faults and hence yielding low terminal reliability. A MIN with redundant paths is then desirable since it can tolerate faults by routing requests over alternative paths and thus achieve enhanced reliability.

The Gamma interconnection network (GIN), proposed by Parker and Raghavendra [4], is one type of MIN composed of $3 \times 3$ switches, with interconnecting patterns between stages following the plus-minus $-2^{i}$ functions. Though able to offer multiple paths from any source to most of the destinations, it provides only a unique path between a source $S$ and a destination $D$

[^0]when $S$ equals $D$, and all the multiple paths existing between certain ( $S, D$ ) pairs share a single common route for many stages before starting to fork, making it impossible to tolerate faults. This leads to one question: Can the GIN be made fault-tolerant without increasing its hardware complexity or even with its cost reduced, to achieve a new network with high reliability? The topic has induced quite a few researchers to come forth with various conclusions. For instance, the Extra stage Gamma network (proposed by Lee and Hegazy [5]) and the PM22I interconnection network (by Lee and Yoon [6]), employing Adams and Siegel's ideas [7], add an extra stage to the GIN to build up multiple paths, but have generated even higher hardware complexity which is quite unfeasible for a GIN whose hardware complexity is already conspicuous. Other than these, the Monogamma network, another modified GIN proposed by Raghavendra and Parker [8], has the hardware complexity no more than the GIN but is able to provide multiple paths between each ( $S, D$ ) pair. However, those multiple paths are not necessarily disjoint that when an internal switch fails, certain source and destination may not be able to communicate with each other.

In this paper, we consider modifications to the GIN by altering the interconnecting patterns between stages so that a modified GIN provides alternative paths between every ( $S, D$ ) pair, including the case when $S=D$. Such a network is referred to as a Cyclic Gamma Intercomection Network (CGIN) as its connecting patterns between stages exhibit a cyclic feature. It should be emphasized that all types of CGINs have totally disjoint paths from any source to any destination, making it possible to tolerate any arbitrary single fault. Besides, if several building blocks (i.e., $3 \times 3$ switches) are fabricated in one chip with VLSI technology, the CGIN enjoys potential cost reduction since its pin count and layout area are less than its GIN counterpart.

## 2. Background

In the following, we briefly review various MINs related to our research.

## Gamma Interconnection Networks

A GIN with size $N=2^{n}$ consists of $n+1$ stages, with each stage involving $N$ switches [4]. Every switch at intermediate stages is a $3 \times 3$ crossbar, whereas the two switches at the first and last stages are of sizes $1 \times 3$ and $3 \times 1$ respectively. The $N$ sources are numbered from 0 to $N-1$, starting with the top one; so are the $N$ switches at each stage and the $N$ destinations. The stages are numbered from 0 to $n$ rightwards. Connecting patterns between stages are based on the plus-minus- $2^{i}$ functions, namely, the $j^{\text {th }}$ switch at stage $i, 0 \leq i \leq n$, is connected to three switches at stage $i+1$ according to the functions: $f_{i}^{p}(j)=j+2^{i}(\bmod N), \quad f_{i}^{m}(j)=j-2^{i}(\bmod N), \quad$ and $f_{i}^{S}(j)=j$, which define the lower, the upper, and the straight connections originating from switch $j$ at stage $i$. A GIN with size 16 is depicted in Fig. 1.

A request from source $S$ in a GIN of size $N=2^{n}$ (denoted by $\mathrm{GIN}_{n}$ ) can be routed to its destination $D$ under the guidance of an $n$-digit tag, which represents the difference (modulo $N$ ) between $D$ and $S$. Each tag digit can be 1,0 , or -1 , and digit $d_{i}$ is used at stage $i$ in a way that the lower (or upper) connection is taken if $d_{i}$ equals 1 (or -1 ), and the straight connection is taken when $d_{i}$ is 0 . For the sake of convenience, -1 is denoted by $\hat{1}$. The GIN makes use of the binary fully redundant number system to represent each tag $T=D-S(\bmod N)$. With this number system, a tag $T \neq 0$ has multiple representations, corresponding to multiple paths in the GIN. As an example, $000 \hat{1}, 00 \hat{1} 1$, 0111 and $\hat{1} 111$ all represent the same value and correspond to four possible paths, say, from source 1 to destination 0, illustrated in Fig. 1.

For a given $N=2^{n}$, there are $3^{n}$ different tag representations since the tag consists of $n$ digits. The tag values lie in the range from $-(N-1)$ to ( $N-1$ ), and the values $(i-N)$ and $i$ are equivalent. In Fig. 1, for example, $T=-1=(15-16)$ has an equivalent tag value of 15 , which can be denoted by 1111 ; the path corresponding to this tag value from source 1 to destination 0 is also provided. The numbers of alternative paths in $\mathrm{GIN}_{4}$ are listed in Table I. As can be seen, there is only a unique path for tag $=0$, and, for certain tag values, the number of alternative paths is small. For instance, when $T$ equals $N / 2$, there are only two alternative paths and when $T$ is $N / 4$ or $3 N / 4$, only three. (Notice that this fact holds for any sized GIN.) Moreover, these alternative paths share the same common route before starting to fork at a later stage. To give an example, the alternative paths between $(6,14)(T=N / 2$ $=8$ ) share the same common route before starting to fork at stage 3 as shown in Fig. 1.

## Monogamma Interconnection Networks

The Monogamma Interconnection Network (MGIN) is constructed from a GIN with the last stage removed and one stage added at the input side; the connecting pattern between the added stage and stage 0 is identical to that between stages 0 and 1 [8]. An MGIN with size 16 is shown in Fig. 2. Its numbers of alternative paths are listed in Table I. As it shows, though there exist multiple paths between any source-destination pair in the MGIN, they are not necessarily disjoint. Take tag $=7$ as an instance (shown in Fig. 2 for the (3, 10) pair). Two alternative paths exist and after the first three stages, both paths share the same common route, unable to guarantee reliable communication between every source-destination pair with the tag.

## 3. Cyclic Gamma Interconnection Networks

For an $n$-stage GIN, the connecting patterns between stages (based on the plus-minus- $2^{i}$ functions) can be ordered as $2^{0}, 2^{1}, 2^{2}, \cdots, 2^{n-1}$, while for an $n$ stage MGIN, it is $2^{0}, 2^{0}, 2^{1}, 2^{2}, \cdots, 2^{n-2}$ (as has been mentioned). With such a slightly different connecting pattern (and with its hardware cost no more than the GIN's), the MGIN is able to provide multiple paths between any source-destination pair. These paths, however, are not necessarily disjoint. To improve it, we move the added stage of the MGIN to the last, that is, changing the connecting patterns into $2^{0}, 2^{1}, 2^{2}, \cdots, 2^{n-2}, 2^{0}$ ( $2^{0}$ for both the first two and the last two stages). By such modification, we obtain multiple paths between any source-destination pair and they are all disjoint. This interesting finding reveals that the connecting patterns between the first two and the last two stages can be any power of 2 , while the connecting patterns between the other stages depict a cyclic feature. Thus we have a new network - the Cyclic Gamma Interconnection Network, or briefed as CGIN.

A modified MGIN with its added stage being moved to the last and its connecting patterns thus being $2^{0}, 2^{1}, 2^{2}, \cdots, 2^{n-2}, 2^{0}$ can be depicted as CGIN $_{n}^{0}$ - $n$ shows an $n$-stage CGIN with size $N=2^{n} ; 0$ indicates the connecting pattern between the first two and last two stages being $2^{0}$. That is, a CGIN $n_{n}^{\gamma}$ refers to a CGIN with $n$ stages, and the connecting patterns between its first two and last two stages being $2^{\gamma}, 0 \leq \gamma \leq n-2$. Thus, the connecting patterns can be ordered as $2^{\gamma}, 2^{\gamma+1}, 2^{\gamma+2}, \cdots, 2^{n-3}, 2^{n-2}, 2^{0}, 2^{1}, \cdots, 2^{\gamma-1}, 2^{\gamma} —$ exhibiting a cyclic feature between stages (i.e., put $2^{0}, 2^{1}, 2^{2}, \cdots, 2^{n-2}$ in order into a circle and then tear apart from $2^{\gamma}$ ). In general, the stages of a $\mathrm{CGIN}_{n}^{\gamma}$ are numbered left to right from 0 to $n$ and the connecting patterns between stages are based on the plus-minus$2^{(\gamma+i) \bmod (n-1)}$ functions. Namely, the $j^{t h}$ switch at stage $i, 0 \leq i<n$, is connected to three switches at stage $i+1$ according to the three functions:
$f_{i}^{p}(j)=j+2^{(\gamma+i) \bmod (n-1)}(\bmod N)$,
$f_{i}^{m}(j)=j-2^{(\gamma+i) \bmod (n-1)}(\bmod N)$, and $f_{i}^{s}(j)=j$, which respectively define the lower, upper, and straight connections originating from switch $j$ at stage $i$. For example, a $\mathrm{CGIN}_{4}^{0}$ and a $\mathrm{CGIN}_{4}^{1}$ are depicted in Fig. 3.

Each request in a CGINn ${ }_{n}^{\gamma}$ also carries a routing tag of $n$ digits, with eacn digit equal to $\hat{1}, 0$, or 1 , and the tag value is the difference between destination and source. The weight of every tag digit is determined by the connecting patterns. Specifically, the $i^{\text {th }}$ tag digit, $d_{i}$, has the weight of $-2^{(\gamma+i) \bmod (n-1)}(\bmod N)$ if $d_{i}$ is $\hat{1}$; it has the weight of $2^{(\gamma+i) \bmod (n-1)}(\bmod N)$ when $d_{i}$ equals 1. That is, the tag is represented by means of a "modified" binary redundant number system. Digit $d_{i}$ is used at stage $i$ when routing the request through a CGIN: it takes the lower (or upper) connection for $d_{i}=1$ (or $\hat{1}$ ), and the straight connection for $d_{i}=0$. Routing complexity is exactly the same in a CGIN as in its GIN counterpart.

It is interesting to find out the number of redundant paths from source $S$ to destination $D$ in a $\operatorname{CGIN}_{n}^{\gamma}$. Since switch $D$ at stage $n$ is connected to three switches $D+2^{\gamma}(\bmod N), D$, and $D-2^{\gamma}(\bmod N)$ at stage $n-1$, a path can reach $D$ through any of these three switches. As a result, the number of alternative paths between $S$ and $D$ turns out to be the sum of all possible paths from $S$ to these three switches, which can be estimated by using the same formula developed for the GIN [4] because the connecting patterns from stage 0 to stage $n-1$ for $\mathrm{CGIN}_{n}^{\gamma}$ is obtained from a permutation of those patterns of the GIN. The number of alternative paths in a $\mathrm{CGIN}_{4}$ for every tag under various $\gamma$ values is provided in Table I. As can be seen, the number of paths between every ( $S, D$ ) pair in any $\mathrm{CGIN}_{4}$ is greater than or equal to 2 , that is, multiple paths always exist from any $S$ to any $D$ in a CGIN. Note that $\mathrm{CGIN}_{4}^{0}$ has exactly the same number of alternative paths as $\mathrm{MGIN}_{4}$ for every tag. However, as Fig. 2 shows, the alternative paths are not necessarily disjoint for $\mathrm{MGIN}_{4}$, like the two alternative paths between $(3,10)($ tag $=7)$. As for $\operatorname{CGIN}_{4}^{0}$ and $\mathrm{CGIN}_{4}^{1}$ (Fig. 3), there are respectively two and three disjoint paths between ( 3,10 ). The fact that there are at least two disjoint paths existing among the alternative paths for every tag in all types of CGINs will be given in the next section.

Evaluating the Pin Count Suppose that $r(r>1)$ rows of switches in a network are fabricated in one single chip. There are $r$ switches in stage $i$ of the GIN housed in a chip, and those $r$ switches connect to $\zeta=2 \times \min \left(2^{i}, r\right)$ switches of stage $i+1$ which locate outside the chip. The pin count contributed by the connections originating from stage $i$ and terminating at stage $i+1$ is thus equal to $\zeta$, where $\min$ is the minimum function. Likewise, the $r$ switches at stage $i+1$ need to
connect $\zeta$ switches of stage $i$ which locate outside the chip, contributing $\zeta$ to the pin count. The number of total pins needed for connections per chip for $\mathrm{GIN}_{n}$ is $2 r+4 \times \sum_{i=0}^{n-1} \min \left(2^{i}, r\right)$, where the first term accounts for the connections for $r$ sources and $r$ destinations.

In general, it is easy to derive that, for any modified GIN with connecting patterns between stages based on the plus- $\rho-$ minus $-\mu$ functions, the amount of total pins for connections per chip is $2 r+2 \times \sum_{i=0}^{n-1} \min (\rho, r)+2 \times \sum_{i=0}^{n-1} \min (\mu, r)$. A pin count saving always results for the CGIN compared with its GIN counterpart, and the saving increases as $r$ grows. The saving is non-negligible. For example, when four rows of switches in Fig. 3(a) (inside a dashed rectangle) are housed in a single chip, that is, when $r$ equals 4,52 pins per chip are needed for $\mathrm{GIN}_{4}$, but only 40 are required for $\mathrm{CGIN}_{4}^{0}$, and the less area is taken by connections of the CGIN between the last two stages (due to the connecting pattern altered from $2^{n-1}$ to $2^{0}$ ). The pin saving coupled with shrunk layout area for connections in a CGIN could translate to cost reduction, making the CGIN practically attractive.

## 4. Proof of Existing Multiple Disjoint Paths

Observing the alternative paths in a CGIN ${ }_{n}^{\gamma}$, we have the following theorem.

Theorem: Consider the alternative paths in a CGIN ${ }_{n}^{\gamma}$. There exist at least 2 disjoint paths (i.e., paths with no internal switch in common) between any pair of source and destination.

Proof: Suppose $\delta$ represents the tag value for paths from source $S$ to destination $D$ in a $\mathrm{CGIN}_{n}^{\gamma}$. As mentioned, a path going through any of the three switches, $D+2^{\gamma}(\bmod N), D$, or $D-2^{\gamma}(\bmod N)$, at stage $n-1$ can reach destination $D$. It is easy to see that the tag values from $S$ to the three switches are $\delta+2^{\gamma}, \delta$, and $\delta-2^{\gamma}$, respectively. Now, two cases are to be discussed.

Case 1. There is a path between source $S$ and switch $D$ at stage $n-1$.
Clearly, $\delta$ is the tag value for the path and $\delta=D-S$. For any ( $n-1$ )-digit tag of value $\delta$, the $0^{2 h}$ digit, $d_{0}$, can be $\hat{1}, 0$, or 1 .
(a) For an ( $n-1$ )-digit tag, say $\tau_{1}$, of value $\delta$ with $d_{0}=\hat{1}$, there exists an $(n-1)$-digit tag, say $\tau_{1}{ }^{\prime}$, of value $\delta+2^{\gamma}$ with the same digits as $\tau_{1}$ except $d_{0}$ which is 0 . Thus, two disjoint paths from $S$ to $D$ through switches $D$ and $D+2^{\gamma}(\bmod N)$ at stage $n-1$ (with tag $0 \tau_{1}$ and tag $\hat{1} \tau_{1}{ }^{\prime}$ ) can be found.
(b) For an ( $n-1$ )-digit tag, say $\tau_{2}$, of value $\delta$ with $d_{0}=0$, there exist an ( $n-1$ )-digit tag, say $\tau_{2}{ }^{\prime}$, of value $\delta-2^{\gamma}$
and an ( $n-1$ )-digit tag, say $\tau_{2}{ }^{\prime \prime}$, of value $\delta+2^{\gamma}$, both having the same digits as $\tau_{2}$ except their $d_{0}$ 's which are $\hat{1}$ and 1 respectively. Thus, three disjoint paths from $S$ to $D$ through switches $D, D-2^{\gamma}(\bmod N)$, and $D+2^{\gamma}(\bmod N)$ at stage $n-1$ (with tags $0 \tau_{2}, 1 \tau_{2}{ }^{\prime}$, and $\hat{1} \tau_{2}{ }^{\prime \prime}$ ) can be found.
(c) For an ( $n-1$ )-bit tag, say $\tau_{3}$, of value $\delta$ with $d_{0}=1$, there exists an ( $n-1$ )-digit tag, say $\tau_{3}{ }^{\prime}$, of value $\delta-2^{\gamma}$ with the same digits as $\tau_{3}$ except $d_{0}$ which is 0 . Thus, two disjoint paths from $S$ to $D$ through switches $D$ and $D-2^{\gamma}(\bmod N)$ at stage $n-1$ (with $\operatorname{tag} 0 \tau_{3}$ and tag $1 \tau_{3}{ }^{\prime}$ ) can be found.

Thus, there exist at least 2 disjoint paths between any pair of source and destination when switch $D$ at stage $n-1$ can be reached from $S$.
Case 2. There is no path between switch $D$ at stage $n-1$ and source $S$.
It is observed that switch $D$ at stage $n-1$ cannot be reached from $S$ only if the tag value, $D-S(\bmod N)$, is $2^{n-1}$. When $\delta=2^{n-1}$, that is, when there is no path between switch $D$ at stage $n-1$ and source $S$, it is easy to derive two ( $n-1$ )-digit tags of values $\delta-2^{\gamma}$ and $\delta+2^{\gamma}$, one with the least significant $n-\gamma-1$ digits being 1 's, the other with the least significant $n-\gamma-1$ digits being $\hat{1}$ 's (the rest of digits for both are 0 's). Obviously, the two tags correspond to two disjoint paths from $S$ to switches $D-2^{\gamma}(\bmod N)$ and $D+2^{\gamma}(\bmod N)$ at stage $n-1$. Thus, two disjoint paths from $S$ to $D$ respectively through the above two switches at stage $n-1$ can be found.

The theorem is thus proved (based on the above two cases).

Let's take $\operatorname{CGIN}_{4}^{0}$ as an example to illustrate the above proof. First, for Case 1(a), two disjoint paths with tags $000 \hat{1}$ and 1000 (through switches 2 and 3 at stage 3) can be found when $S=3$ and $D=2$. For Case $l(b)$, when $S=3$ and $D=5$, three disjoint paths in existence are with tags 0010, $101 \hat{1}$ and $\hat{1} 011$ (through switches 5 , 4 and 6 at stage 3). When $S=3$ and $D=8$, the two disjoint paths to be found for Case I(c) carry tags 0101 and 1100 (through switches 8 and 7 at stage 3). As for Case 2, when $S=3$ and $D=11$, the two disjoint paths found are with tags 1111 and $\hat{1} 1 \hat{1} \hat{1}$ (through switches 10 and 12 at stage 3 ).

## 5. Terminal Reliability Evaluation

The terminal reliability between a sourcedestination pair in a MIN is the probability that at least one path exists between the pair. For any tag in the GIN, all the alternative paths may be represented by a simple ladder diagram [4], but it is not the case with the CGIN. The alternative paths in a CGIN no longer constitute a simple structure, making the derivation of an
exact expression for the terminal reliability seems fairly complicated. In search of an efficient method able to evaluate the terminal reliability of a CGIN, we have reviewed several related algorithms in the literature and come forth with a simple approach [9] able to evaluate the terminal reliability of any MINs.

The simple approach has been employed to calculate the terminal reliabilities for CGIN ${ }^{\prime}$ 's (where $0 \leq \gamma \leq 2$ ) and CGIN ${ }^{\gamma}$ 's (where $0 \leq \gamma \leq 4$ ). The results are almost identically good as what is reported here for $\mathrm{CGIN}_{4}^{0}$ and $\mathrm{CGIN}_{6}^{0}$ whose terminal reliabilities versus tag are plotted in Figs. 4 and 5 (note that the reliabilities of a $3 \times 3$ switch is assumed to be 0.9 ; the $1 \times 3$ and $3 \times 1$ switches at stage 0 and $n$ are fault-free). For easy comparison, the terminal reliabilities for GIN and MGIN with system sizes 16 and 64 are also plotted in both figures. As expected, a CGIN enjoys much enhanced terminal reliability, whereas the GIN suffers relatively low values, and the contrast is remarkable. To give an example, when the tags are 8 and $32(=N / 2)$ respectively in size 16 and 64 networks, GIN experiences the lowest value (as when the tag is 0 ), while the values for CGIN remain impressively high, thanks to the existence of its multiple disjoint paths. It is also worth our attention that for a GIN with tags 7 and 9 in a size 16 network or 31 and 33 in a size 64 network, its reliability stands higher than CGIN. This is because there are two disjoint paths among the 7 and 11 alternative paths for each case. As for MGIN, since its multiple paths are not necessarily disjoint, it fails to have as high reliability as CGIN in almost all cases except on tags 8 (system size 16) and 32 (system size 64) where both networks display the same values, leading us to the fact that MGIN has disjoint paths on both tags. Clearly enough, it is of much significance for all various networks to have multiple disjoint paths, like our CGINs, to ensure constant and satisfactorily high terminal reliabilities.

## 6. Experimental Performance Evaluation

The performance results of various CGINs under different network parameters are obtained through simulation for comparison. A network under simulation operates in a packet-switched mode, where every request involves only a single packet and is routed according to the strategy mentioned in Section 3. Each request in a network of size $2^{n}$ carries a routing tag of $n$ digits, and the tag is selected randomly from all possible tag representations for the tag value of the request. At every network input, a table is used to store all possible tag representations of each tag value, and when a request is generated, the table is looked up for selecting a tag representation; each possible representation of a given tag value has the same probability of being selected.

A simulated network is assumed to be synchronous, with the network cycle being the smallest time unit in which a request can be transmitted from one switching element to another. The assumptions in [10] are followed in our simulation, and the same measures of interest, bandwidth and mean delay, are adopted in this experimental study. Bandwidth is the average number of requests accepted at each network output per cycle. Mean delay indicates the number of network cycles spent by a typical request from its source to its destination; the delay of a request is counted from the time the request is generated (rather than from the time it is admitted to the network) until it leaves the network. The results collected from our simulation are depicted in Figs. 6 and 7, where every point given represents a steady state result. Note that bandwidth, though a collected measure under various request arrival rates, is chosen as one axis for plotting delay-bandwidth characteristics in the figures.

Mean delay versus bandwidth of various CGIN ${ }_{n}^{\gamma}$ 's with fixed queue capacity $\eta=2$ is shown in Fig. 6 for different network sizes $2^{n}, n=4,5$, and 6 . (It is assumed in [10] that a queue with capacity $\eta$ is associated with every switch output port and each network input.) For each $n$, all CGIN $_{n}^{\gamma}$ 's with $\gamma$ ranging from 0 to $n-2$ are simulated and the results are provided in the figure. As can be seen, all $\mathrm{CGIN}_{n}^{\gamma}$ 's exhibit virtually identical delay-bandwidth characteristics for any given $n$. The simulation results of $\mathrm{GIN}_{n}$ are included in the figure (shown by dotted curves) for comparison. It is observed that a $\operatorname{CGIN}_{n}^{\gamma}$ and its $\operatorname{GIN}_{n}$ counterpart have about the same performance, with the difference falling within tolerable simulation accuracy. This reveals that altering the interconnecting patterns between GIN stages leads to no performance loss, despite a significant gain in terminal reliability and possible cost reduction. It is interesting to notice in the figure that the performance gaps between different sized networks remain unchanged for bandwidth up to roughly 0.7 , at which point networks are not heavily loaded yet. The gaps are attributed to the different numbers of stages requests travel in different sized networks. When the network load becomes heavy, the queuing delay in each stage grows substantially and the performance gaps between different sized networks change.

The performance of $\mathrm{CGIN}_{6}$ with various queue capacities is illustrated in Fig. 7. Since all CGIN ${ }_{6}$ 's, $0 \leq \gamma \leq 4$, possess virtually the same performance, only the result of $\operatorname{CGIN}_{6}^{0}$ is given for clarity. It can be seen that a CGIN with queue capacity $\eta$ equal to 3 can deliver performance close to that of a CGIN with infinite queue capacity. Compared with $\mathrm{GIN}_{6}$ (shown by dotted curves), CGIN ${ }_{6}^{\gamma}$ again has almost identical performance for any given queue capacity.

## 7. Concluding Remarks

In this paper, we have investigated "modified" Gamma intercomnection networks obtained by altering the connecting patterns between certain consecutive stages of the GIN. A new modified network exhibiting a cyclic feature of its connecting patterns between stages has been initiated and is dubbed as a CGIN. It exhibits high terminal reliability compared with GIN and MGIN, another modified GIN, because any type of CGINs can guarantee the existence of totally disjoint paths between any communication pair, For CGIN and its GIN counterpart, the routing complexity stands the same. All the paths from any source to any destination in a CGIN can be represented by a "modified" binary redundant number system. If several rows of switching elements are fabricated in one chip using the VLSI technology, a CGIN could lead to reduced cost because the pin count per chip decreases and the layout area taken by connections shrinks. It is found through simulation that CGIN delivers virtually identical performance as GIN. REGIN, another modified GIN built also by altering the connecting patterns of GIN to create disjoint paths between each source-destination pair, has been reported recently in [10]. However, only one type of the REGINs has multiple disjoint paths between every $(S, D)$ pair, and the pin count is not reduced so much as the CGINs. Moreover, characterized by plus- $\rho-$ minus $-\mu$ functions where $\rho=\mu$, the connecting pattern for CGIN, like for GIN, is symmetric, while the REGIN's is without symmetry ( $\rho \neq \mu$ ). We thus believe it is feasible for CGIN to adopt destination tag routing and rerouting [11] - which is currently under investigation.

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Table I. The number of alternative paths for every tag in a network with size 16

| Tag | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| :--- | ---: | ---: | ---: | ---: | ---: | ---: | ---: | ---: | ---: | ---: | ---: | ---: | ---: | ---: | ---: | ---: |
| GIN $_{4}$ | 1 | 5 | 4 | 7 | 3 | 8 | 5 | 7 | 2 | 7 | 5 | 8 | 3 | 7 | 4 | 5 |
| MGIN $_{4}$ | 7 | 6 | 8 | 6 | 6 | 4 | 4 | 2 | 2 | 2 | 4 | 4 | 6 | 6 | 8 | 6 |
| CGIN $_{4}^{0}$ | 7 | 6 | 8 | 6 | 6 | 4 | 4 | 2 | 2 | 2 | 4 | 4 | 6 | 6 | 8 | 6 |
| CGIN $_{4}^{1}$ | 5 | 9 | 4 | 8 | 4 | 6 | 2 | 4 | 2 | 4 | 2 | 6 | 4 | 8 | 4 | 9 |
| CGIN $_{4}^{2}$ | 3 | 8 | 5 | 7 | 2 | 6 | 4 | 6 | 2 | 6 | 4 | 6 | 2 | 7 | 5 | 8 |

(The number of total paths amounts to $3^{4}=81$ in every network.)


Fig. 1. A Gamma interconnection network with size 16. (Bold lines indicate alternative paths between ( 1,0 ) and between ( 6,14 ).


Fig. 2. A Monogamma interconnection network with size 16. (Bold lines indicate altemative paths between $(3,10)$.)



Fig. 5. Terminal reliability comparison among $\operatorname{GIN}_{6}, \mathrm{MGIN}_{6}$, and $\mathrm{CGIN}_{8}^{9}$.


Fig. 6. Mean delay versus bandwidth of various CGIN\%'s with queue capseity $\eta$ equal to 2 .
(The $\mathrm{OiN}_{n}$ renults are atown by doted curves.)


Fig. 7. Mean delay versus bandwidth of CGIN? for various queue capacities.
(The GIN $_{6}$ results are shown by doted curves. The number at the end of each curve indicates queue capacity $\eta$.)


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