

Hardware/Software Co-design of Particle Filter and Its Application in Object Tracking

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Abstract—This paper presents a hardware/software co-design method for particle filter based on System On Program Chip (SOPC) technique. Considering both the execution speed and design flexibility, we use a NIOS II processor to calculate weight for each particle and a hardware accelerator to update particles. As a result, execution efficiency of the proposed hardware/software co-design method of particle filter is significantly improved while maintaining design flexibility for various applications. To demonstrate the performance of the proposed approach, a real-time object tracking system is established and presented in this paper. Experimental results have demonstrated the proposed method have satisfactory results in real-time tracking of objects in video sequences.

Keywords- *particle filter; FPGA; object tracking; SOPC; HW/SW co-design;*

I. INTRODUCTION

As an effective tool for estimating system states, particle filters based on Bayesian approach [5] use authentic information to establish posterior Probability Density Function (PDF) [6],[7] to estimate the state model [8]. Because of its effectiveness, the particle filter [3],[4] has been widely used for solving problems with high dimensions for non-linear systems. However, one of the disadvantages of the particle filter is the complexity involved, particularly, for real-time embedded applications because complex mathematical operations of the particle filter will inevitably involved during each iteration. When the quantity of the particles increases, memory usage and computational effort increase accordingly, resulting in poor performance of the particle filter.

As an attempt to solve the above-mentioned problem, this paper presents a hardware/software co-design [22] approach to realize the particle filter using a SOPC-based approach [20],[21]. Because of hardware acceleration with limited usage of resources, execution speed of the proposed approach is much faster than that of pure software realization of particle filter. Also, hardware does not have to undergo redesign for various applications because of design flexibility of the proposed approach. Based on a proposed framework of the hardware/software co-design method, weight of the particles is calculated on the Nios II processor in this paper, while a FPGA hardware circuit is designed as an accelerator to update

particles. As a result, calculation burden of the Nios II processor can be significantly decreased. In conventional particle filter algorithm, resampling is a very important step, which affects the distribution of the particles in the next generation. Traditional particle filters generally use the Stochastic Universal Sampling method [27] as the resampling mechanism, where particles with high weight are statistically selected many times. This leads to a loss of diversity among the particles as the resultant sample will contain many repeated points. This problem, which is known as sample impoverishment, is severe in the case of small process noise [28]. To address this problem, we will introduce the concept of tournament selection [19] widely used in genetic algorithm as the resampling mechanism, where a tournament size can be used to determine the selectivity pressure to choose particles from the current population. By doing so, floating-point operation of weight calculation of the particles in the design of hardware circuit can be avoided, thus improving the performance of the particle filter.

To demonstrate the effectiveness of the proposed approach, a real-time object tracking system is proposed in this paper, where a multi master-slave system architecture is adopted to effectively improve the system performance in image capturing and display. Together with the hardware/software co-design with the use of a particle filter circuit, the proposed framework reduces the resources required during the computation while providing design flexibility for real-time object tracking in video sequences.

II. PARTICLE FILTERS

Particle filter methods, particularly the sampling importance resampling (SIR) algorithm [2], are Monte Carlo (MC) methods that implement a recursive Bayesian filter by MC simulations. The key idea of particle filter methods is to represent the required posterior probability density function (pdf) by a set of random samples $X_k = \{x_k^1, x_k^2, \dots, x_k^m\}$ with associated weights w_k^m to compute estimates based on these samples and weights, where m is the number of samples and k is the sample time. As the number of samples becomes very large, this MC characterization becomes an equivalent representation to the usual functional description of the posterior pdf [1], and the SIR filter approaches the optimal

Bayesian estimate. Essentially, a typical particle filter includes three computational steps:

A. Weight Calculating

Utilize measurement information z_k and particle x_k^m to calculate weight w_k^m associated with each particle x_k^m as a probability:

$$w_k^m = p(z_k | x_k^m) \quad (1)$$

These weights are then normalized by the sum over all particle weights to obtain the posterior distribution.

$$w_k^m = \frac{w_k^m}{\sum_{i=1}^m w_k^i} \quad (2)$$

B. Resampling

The tournament selection widely used in genetic algorithm is adopted in this paper to avoid the problem of sample impoverishment, where a tournament size “ K ” can be used to determine the selectivity pressure to choose particles from the current population. By doing so, we can draw particles from x_k^m according to the weight w_k^m .

C. Prediction

Draw samples x_k^m from state transition probability $p(x_k | u_k, x_{k-1}^m)$ conditioned on x_{k-1}^m at time k and control command u_k .

III. HARDWARE/SOFTWARE CO-DESIGN OF PARTICLE FILTER

Figure 1 shows a framework based on a hardware/software co-design approach for particle filters. We will use this framework to establish a real-time object tracking system.

As mentioned earlier in Introduction, most particle filters involve vast amount of computational complexity, thus resulting in challenges for real-time embedded applications. For example, particle filters implemented in embedded processor, such as Nios II processor, have very slow execution speed. As an attempt to provide design flexibility for various embedded applications and accelerate execution efficiency, a hardware/software co-design method using hardware description language Verilog is proposed in this paper, in which modular design is used to construct the major components, including a Particle Filter Accelerator and a Weight Calculating module. In what follows, we will describe these functional modules in more details.

A. Particle Filter Accelerator

The Particle Filter Accelerator module is a hardware circuit designed to accelerate the execution speed. As shown in Fig. 1, there are five important circuits in the Particle Filter Accelerator module, including (1) Initialization, (2) Particle Update, (3) Random Number Generator, (4) Particle Filter State Machine, and (5) On-chip Memory. Respective functionalities of these modules are described as follows:

1) Initialization module: The Initialization module is used to initialize particles required for the particle filiter. There are three components to achieve this objective, including (a) Boundary Comparison module, (b) State Controller module, and (c) FIFO module.

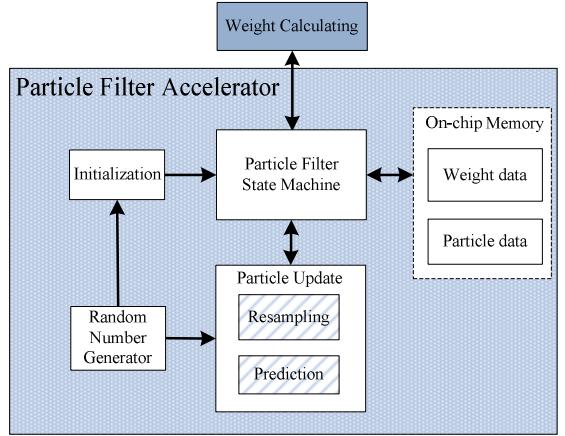


Figure 1. Hardware/software co-design of particle filter.

2) Particle Update module: This module is used to update particle data. This module is used to process the resampling and prediction steps to generate updated particle for the next gernation. There are three components in this module.

(a) Resampling module:

The Resampling module reads out the particle data and weight data from the Particle Filter State Machine module. Based on a tournament selection mechanism using random data #1, this module generate particles (Temp Particle Data) for use in the prediction step.

(b) Prediction module

The Prediction module generate New Particle Data by adding some random noises from Random Data #2 as perturbations to particles (Temp Particle Data) from the Resampling module. When all particles are generated, they will be trasnferred and saved into the On-chip memory through Particle Filter State Machine.

(c) State Controller #2 module:

This State Controller #2 module is used to control and coordinate the Particle Update module. First, the Resampling module will transfer the partilce data and weight data from Particle Filter State Machine module. And next, the State Controller #2 will wait the Prediction module to complete all particle prediciton. Finally, the State Controller #2 will send the new particle data to the On-chip memory through Particle Filter State Machine.

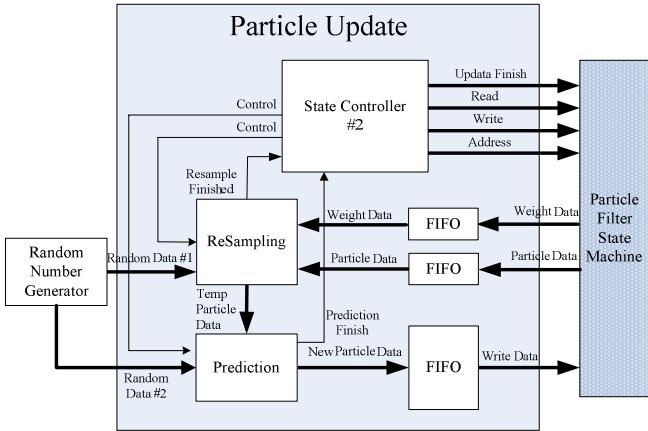


Figure 2. Particle update module.

3) Random Number Generator module: A Keep-It-Simple-Stupid (K.I.S.S) random number generator (RNG) algorithm is implemented [26] in this paper. The idea is to use simple, fast, individually promising generators to get a composite that will be fast, easy to code.

4) *Particle Filter State Machine module*: The Particle Filter State Machine module is designed using state machine to change state for access RAM data. There are three states in this state machine, including the initialization state, weight calculating state, and particle update state.

B. Weight Calculating

Fig. 3 shows the components of the proposed weight calculating module, including a Nios II processor for software weight assignment, a Hardware Weight Assignment Master module, and a Weight Slave. Because various applications need to be dealt with, the weight calculating module should accommodate the diversities of problems, and is therefore preferably implemented by a software module for evaluating weight functions in the first place.

The weight calculating module is designed with multi master-slave architecture, as shown in Fig. 3. Both Nios II processor and Hardware Weight Assignment Master can transfer the weights to Particle Filter Accelerator module by using Weight Slave module. Because Nios II processor can calculate weight by software code, therefore the use of Nios II processor has better design flexibility for various embedded applications. For a particular problem, we can use hardware implementation to speed up execution speed once prototype testing is completed.

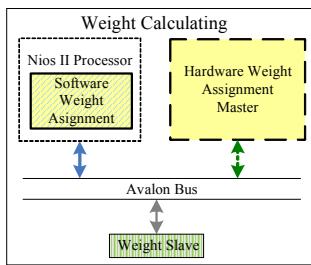


Figure 3. Weight calculating module.

IV. OBJECT TRACKING VIA THE PROPOSED PARTICLE FILTER

Based on a multi master-slave [23] architecture, this paper proposed a SOPC design method to accelerate the processes of image capturing, image display, and object tracking via the particle filter method. The architecture of the proposed real-time object tracking system is shown in Fig. 4.

A. Image capture process

The CMOS Capture module will transfer image data to both the SSRAM and the SDRAM storage via an Avalon bus. The image data in SDRAM will be used to calculate the weight of the particles. The image data stored in SSRAM will be used to display the CMOS original image.

B. Image display process

The LTM Display module will transfer image data from SSRAM to LTM module and mark the object coordinate by a red rectangle on the screen.

C. Image tracking process

For real-time object tracking, each particle represents a coordinate in the image plane. In this paper, a Nios II processor is used to calculate weight associated with a particle. Because image data is very large, which requires significant computation, therefore a hardware circuit to calculate the weight for particles is desired. The weight calculating results will be transferred to the Particle Filter Accelerator module via the Weight Slave module. Finally, the particle with the highest weight value will be chosen and sent to the LTM module to display the object coordinate.

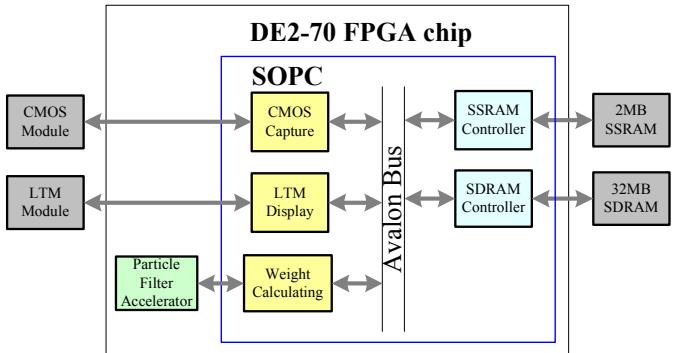


Figure 4. Architecture of the real-time object tracking system.

V. EXPERIMENTAL RESULTS

In this paper, a DE2-70 development board by Altera [25] is used as an experiment platform for evaluating the performance of the proposed approach. We will compare the performance of particle filter implemented by both hardware and software design methods, followed by experiments of the proposed object tracking system, where a red ball is the object to be tracked. A set of 32 particles is used in the particle filter.

A. Performance of the Particle Filter Accelerator

TABLE I shows the time elapsed for two major computational steps of the particle filter via hardware and software implementation to search and track a red object. It is clear that hardware circuit has far better performance than software implementation. A speedup up to 7000 times can be obtained by using the Particle Filter Accelerator. However, hardware circuit design is more difficult than software realization. Therefore, we can use hardware/software co-design method to accelerate execution speed while maintaining design flexibility.

B. Performance of the object tracking system

TABLE II shows the performance of the real-time object tracking system. Two mask size of 32×32 and 64×64 are respectively used to validate the system performance of the particle filter, where weight calculation are implemented by either software and hardware implementation. As demonstrated in this table, a speedup of approximately 4 times can be achieved by the proposed hardware/software co-design method.

VI. CONCLUSIONS

In this paper, a SOPC-based framework for particle filters is proposed. Both Nios II processor as software weight assignment or hardware weight assignment master as a hardware accelerator can be used to calculate weights for the particles. As a result, a balance between execution efficiency and design flexibility of the particle filter can be maintained. In the practical experiment, a multi master-slave architecture is proposed to demonstrate image capturing, display, and object tracking in a video sequences. As demonstrated in the experimental results, the proposed hardware/software code-design method has satisfactory performance for real-time object tracking.

TABLE I. EXECUTION PERFORMANCE OF PARTICLE FILTER

Computational step	Time elapsed (μ s)		Times
	SW	HW	
Initialization	589.568	0.08325	7081.898
Re-sampling and prediction	4511.552	1.7925	2516.9

TABLE II. PERFORMANCE OF REAL-TIME OBJECT TRACKING VIA HW/SW CO-DESIGN

Method	Mask size	Module	Time elapsed (ms)	Iteration (times/s)
HW/SW co-design	32×32	Weight calculation (SW)	19.77598	50
		Particle update (HW)	0.0017925	
	64×64	Weight calculation (SW)	78.323196	13
		Particle update (HW)	0.001785	

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