A Q-band Direct Divide-by-4 Injection-Locked Frequency Divider with Quadrature Outputs

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***Abstract*—A divide-by-4 injection-locked frequency divider is designed for applications in the millimeter-wave frequency range. The proposed circuit also features in quadrature phase outputs by using a quadrature voltage-controlled oscillator. The input signal is injected into the common-mode node at the tail current source directly. Implemented in a 0.13 µm CMOS technology, the core circuit consumes dc power of 3.66mW with 1.2 V supply voltage. The operation range achieves 1.95 GHz. The entire die occupies an area of 974×726 um^2.**

I. INTRODUCTION

For high-speed wireless communication applications, the operating frequency has moved to millimeter frequency bands, such as 60 GHz, to take advantage of large signal bandwidth. The phase-locked loop (PLL) synthesizer is still popularly used to generate LO signals in the RF transceiver. The frequency divider chain consumes large power in order to compare the LO output with a reference signal in the high-frequency PLL. The prescalar at the first stage faces design challenge of high operating frequency and low power consumption.

Two approaches are widely used for frequency divider design. They are the injection-locked frequency divider (ILFD) and current-mode logic based frequency divider (CMLFD). Operated at such a high frequency, the power-hungry CMLFD topology is generally not suitable as the first stage in the divider for millimeter-wave PLL design [1]. For low-power consideration, a frequency divider with a high divide ratio will help reduce the number of circuit blocks and save overall dc power. The block diagram of millimeter-wave PLL is shown in Fig.1. In this work, instead of the typical divid-by-2 circuit, a direct divide-by-4 injection-locked frequency divider is proposed for prescalar application in 0.13 µm CMOS technology. The proposed frequency divider features a divide ratio of four times, low power consumption. The input signal is injected to lock the outputs of a QVCO. As such, quadrature phase outputs are obtained.

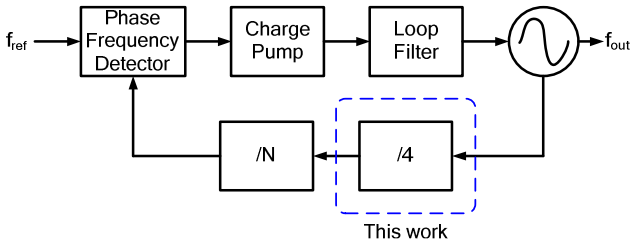

Fig. 1. Block diagram of millimeter-wave PLL.

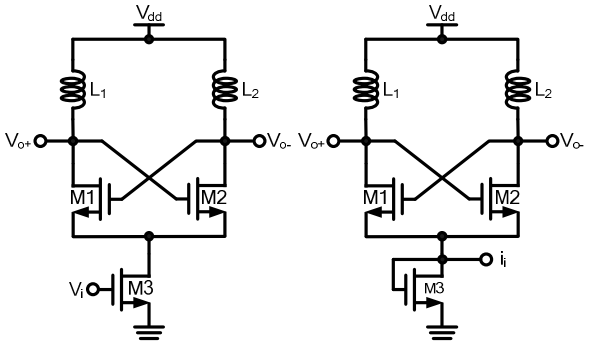

Fig. 2. Schematic of two topologies of the conventional injection-locked frequency divider.

This paper is organized as follows. In Section II, the circuits design considerations are described. The measurement results are shown in Section III. Finally, a conclusion is given in Section IV.

II. CIRCUIT DESIGN

The design of frequency division by injection locking can be illustrated by the divide-by-2 circuits as shown in Fig. 2 [2] [3]. The divider circuit includes an LC oscillator consisting of cross-coupled transistors, M1 and M2. The free-running frequency f_0 of the oscillator is designed near a fraction of the injection signal frequency, $n \times f_0$. To a divid-by-2 circuit, n equals to 2. The input signal is injected into the common-mode node in the oscillator where the frequency component

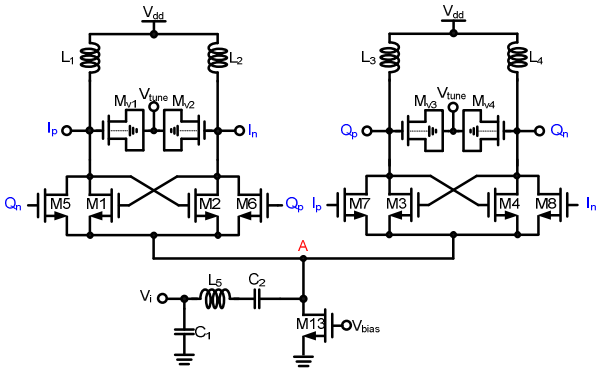

Fig. 3. The schematic of the proposed direct divide-by-4 injection locked frequency divider.

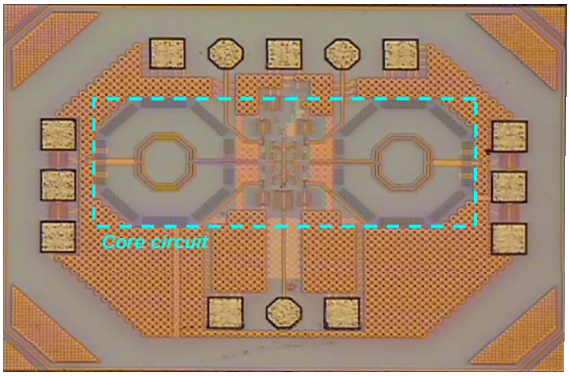

Fig. 4. The micrograph of the fabricated frequency divider.

$2f_0$ resides with the maximum power (f_0 is self-oscillation frequency). The common-mode node could be selected at the location of the tail current source. As such, the oscillator is locked to the half frequency of the injected signal.

The difference between the two topologies in Fig. 2 is described as follows. In Fig. 2(a), M3 is used as a trans-conductor to convert the input voltage swing to an injection current. But the input signal in Fig. 2(b) is directly injected into the common-mode node. M3 is only a tail current source of this oscillator. In millimeter-wave frequency divider design, the circuit in Fig. 2(a) typically consumes more dc power.

The technique of the signal injection at the common-mode node can be extended to divide-by-4 frequency divider circuits. As far as quadrature phase outputs are concerned, a quadrature-phase voltage controlled oscillator (QVCO) is the best candidate for the requirement. The signal outputs of two oscillators are coupled or injected to each other such that the outputs appear to be in quadrature out of phase. The injected node is then to be selected at the circuit node with the maximum power of $4f_0$. If the two oscillators are supplied by the same tail current source, the frequency component of $2f_0$ in each oscillator becomes 180 degrees out of phase and nulls out at the location of the current source, while the component $4f_0$ exists to the maximum level. This circuit node, therefore, meets the design requirement.

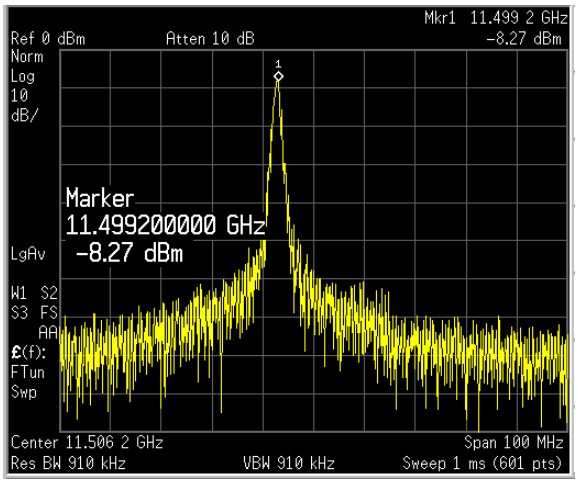

Fig. 5. The measured spectrum under free running at V_{tune}=1.2 V

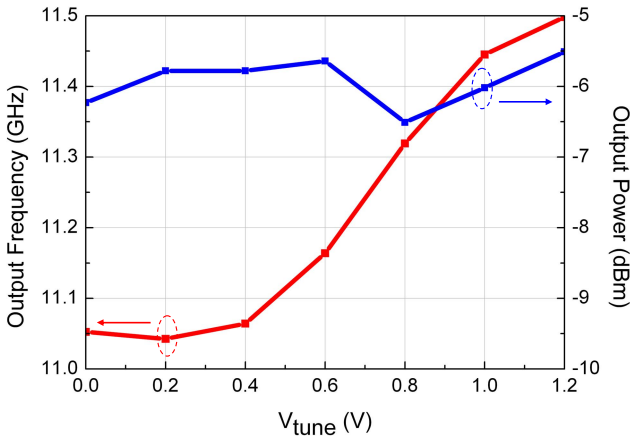

Fig. 6. Measured free-running frequency and output power of the frequency divider along with the tuning control voltage.

Fig. 3 shows the schematic of the proposed direct divide-by-4 frequency divider. M1~M2 and M3~M4 are two pairs of the cross-coupled transistor pair used to provided negative resistance to compensate for the LC tank loss. The LC tank is formed by inductors (L_1~L_4), MOS varactors (Mv1~Mv4) and other parasitic capacitance. The coupling transistors (M5~M8) force the two LC VCOs to lock in quadrature outputs. The source terminals of the two VCOs are connected together at node A to produce maximum $4f_0$. For low power consideration, M9 is designed as a current source to provide dc bias. The input signal is direct injected into the node A. The input matching network is realized by L_5 and C_1. For measurement consideration, the output buffer is carrier out using the open drain topology in this work.

The proposed injection technique is different from that in the circuit with quadrature outputs [5]. In that reference, signal is injected to a transistor acting as a harmonic mixer at the output nodes. Although the locking range could be large if the tank Q is low, the intrinsic function of a mixer generates spurs that appear at the output directly without much filtering by the low-Q tank. On the other hand, the direct common-mode node injection benefits in better spurious noise

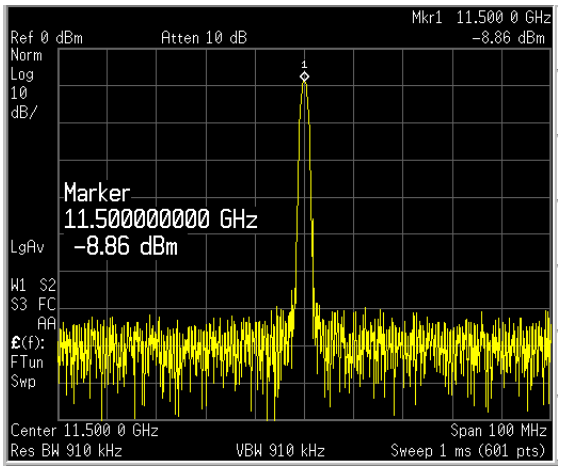

Fig. 7. The measured spectrum of the frequency divider output locked to an input signal of 0 dBm at 46 GHz.

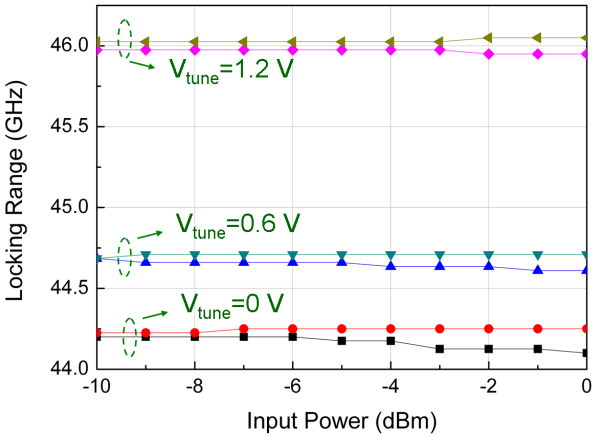

Fig. 8. The measured input locking range versus input power.

performance because only the desired frequency component is found inherently.

III. MEASURMENT RESULTS

The proposed direct divide-by-4 injection-locked frequency divider is designed and fabricated in TSMC 0.13 µm CMOS technology. The divider can generate quadrature outputs. But only two signal output is with the probe pad for on-wafer measurements. The chip micrograph is shown in Fig. 4. The area of the total chip is 974x726 µm^2, while the core circuit occupies 648x252 µm^2. At V_{dd}=1.2 V, the core circuit and buffer dissipate dc power of 3.66 mW and 14.9 mW, respectively.

The display of the spectrum analyser is before calibration of cable loss. The cable loss is about 2.8 dB. Fig. 5 shows the output spectrum of this designed frequency divider free running at V_{tune}=1.2 V, without any input injected signal. The output power is -8.27 dBm. Fig. 6 shows the plots of the free-running frequency and output power measured along with the tuning voltage. With the tuning voltage from 0 to 1.2 V, the output frequency varies from 11.025 GHz to 11.499 GHz.

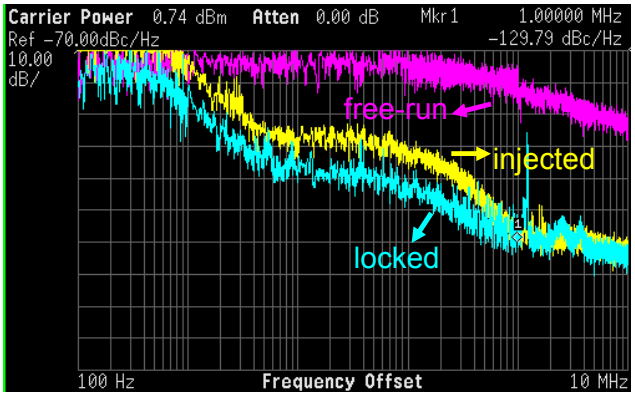

Fig. 9. The measured phase noise of different signals, including the free-running, injected, and locked output signal.

With 0 dBm input power at 46 GHz, the output signal spectrum under the locked condition is shown in Fig. 7.

The measured locking range is shown in Fig. 8. Only three conditions of tuning voltage are plotted. At V_{tune}=0 V with 0 dBm input power, the maximum locking range is 150 MHz. When the self-oscillating frequency is tuned by the MOS varactors, the locking range covers from 44.1 to 46.05 GHz.

Fig. 9 shows the results of phase noise measurements using the same spectrum analyser. Three different signals are recorded for comparison, including the free-running, input injected signal, and output locked signals. At 1-MHz offset frequency, the plot shows the phase noise of -82 dBc/Hz, -126.24 dBc/Hz, and -129.8 dBc/Hz, respectively. Beyond this offset frequency, the phase noise of the injected and the output signals appears to be the same, limited by the spectrum analyser. At lower offset frequencies, it is observed that the phase noise difference between the injected and the output signals is about 10 dB, 2 dB short of the theoretical value.

The circuit performances of the frequency divider are summarized in Table I. Some other references are also listed for comparison. This divider can generate the divide-by-4 output frequency and quadrature outputs with low power consumption.

IV. CONCLUSIONS

A Q-band direct divide-by-4 injection-locked frequency divider with quadrature outputs in 0.13-µm CMOS technology is presented in this paper. The measurement results show that the locking range with tuning is 1.95 GHz. The core circuit draws only 3.66 mW from 1.2 V power supply.

ACKNOWLEDGMENT

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TABLE I.
PERFORMANCE SUMMARY AND COMPARISON.

Ref	This work	[4]	[5]	[6]
V_{dd} (V)	1.2	2	1.2	1.2
V_{tune} (V)	0~1.2	0~1	0.1~1.3	0~1.2
P_{diss}(mW)	3.66	10	7.56	3.12
Free-running frequency (GHz)	11.025 ~11.499	15.37 *	11.5~12.7	1.72~1.99
Output phase	4	2	2	4
P_{in} (dBm)	0	0	> 0	0
L.R. w/o tuning	150 MHz	11 MHz	N/A	N/A
L.R. w/ tuning	1.95 GHz (44.1~ 46.05 GHz)	270 MHz**	5 GHz (45.9~50. 9 GHz)	1.16 GHz (6.86~8.0 2GHz)
Area (μm^2)	Core: 648x252 Total: 974x726	910x1150	350x500	1040x101 0
Process	0.13 µm CMOS	0.18 µm CMOS	0.18 µm CMOS	0.18 µm CMOS

L.R.: locking range
*: tuning range is not shown
**: the boundary of locking range is not shown

REFERENCES

[1] Changhua Cao, Yanping Ding, and Kenneth K. O, "A 50-GHz Phase-Locked Loop in 0.13-µm CMOS," *IEEE J. of Solid-state Circuits*, vol. 42, no. 8, Aug. 2007

[2] Hamid R. Rategh, Thomas H. Lee, "Superharmonic injection-locked frequency dividers," *IEEE J. of Solid-state Circuits*, vol. 34, no. 6, June 1999.

[3] Zue-Der Hung, Chung-Yu Wu, and Bi-Chou Huang, "Design of 24-GHz 0.8-V 1.51-mW coupling current-mode injection-locked frequency divider with wide locking range," *IEEE Trans. Microwave Theory and Tech.*, vol. 57, no. 8, Aug. 2009.

[4] Fan-Hsiu Huang and Yi-Jen Chan, "V-Band CMOS Differential-type Injection Locked Frequency Dividers," International Symposium on VLSI Design, Automation and Test, April 2006.

[5] Mei-Chen Chuang, Jhe-Jia Kuo, Chi-Hsueh Wang, and Huei Wang, "A 50 GHz divide-by-4 injection lock frequency divider using matching method," *IEEE Microwave Wireless Compon. Lett.*, vol. 18, no. 5, May 2008.

[6] Shao-Hua Lee, Sheng-Lyang Jang, and Yun-Hsueh Chung, "A low voltage divide-by-4 injection locked frequency divider with quadrature outputs," *IEEE Microwave and Wireless Compon. Lett.*, vol. 17, NO. 5, May 2007.