Temperature Insensitive Current Reference for the 6.27 MHz Oscillator

Wei-Bin Yang
Dept. of E. E.
Tamkang University
New Taipei City, Taiwan
robin@ee.tku.edu.tw

Zheng-Yi Huang
Dept. of E. E.
Tamkang University
New Taipei City, Taiwan
enjoyable_qq@hotmail.com

Ching-Tsan Cheng
Dept. of E. E.
Tamkang University
New Taipei City, Taiwan
t26213665@yahoo.com.tw

Yu-Lung Lo
Dept. of E. E.
National Kaohsiung Normal University
Kaohsiung, Taiwan
yllo@nknu.edu.tw

***Abstract*—This paper describes a circuit, which generates temperature-independent bias currents. In this paper, low- temperature coefficient reference is presented. The circuit is firstly employed to generate a current reference with temperature compensation, then combining the opposite characteristic curve current reference to minimize the variation of temperature. The proposed circuit has been design by a 0.18um CMOS technology process and using computer simulation to evaluate the thermal drift of the reference current. This current reference is used to provide a stable current for a current controlled oscillator(CCO). The proposed CCO achieves temperature coefficients of 22.3 ppm/℃ in the temperature range between -25 and 75℃.**

Keywords- ***current reference, ring oscillator***

I. INTRODUCTION

Current and voltage references are indispensable circuit in analog, digital and power electronic systems. These should be designed stable as possible, the current and voltage references with high temperature immunity for proper operation. They are usually used to determine biasing points of sensitive analog circuits, for example amplifiers, oscillators, phase-locked loops (PLLs). Many high precision, temperature-independent reference circuits have been designed in the document over the last decades [1]-[3], many approaches have been made in order to design reliable current and voltage references in CMOS technology process.

Many CMOS current and voltage references consists of bipolar junction transistors (BJTs), which have been adapted to CMOS exploiting the parasitic lateral bipolar junction transistors in CMOS processes [4]-[5]. In addition, all-MOS voltage references have been proposed which use the thermal properties of MOS transistors worked in weak inversion region [6]or, recently the threshold voltage compensate the mobility temperature drift [7]-[11]. However, current references having MOS transistors operating in this region tend to have fairly large temperature coefficients. In these solutions, the circuits which want to obtain good temperature performance are complex and require a large area [12]-[14].

There is a design of current-controlled oscillator (CCO) in the following. To achieve the goal of compensating the frequency of CCO, an independent of temperature current reference is needed. When the proper current reference is brought in to the current-controlled oscillator, the frequency of CCO is compensated as following.

In this paper, the proposed circuit introduces a low-TC CMOS current reference utilizing MOS transistors operating in the weak inversion region and the current-controlled oscillator is compensated by the proper reference. The rest of this paper is organized as follows. Analysis for the proposed CMOS reference and current-controlled oscillator are both described in section II. Section III presents simulation results of several voltage and current references and oscillator to assess the performance. Finally, conclusions are given in Section IV.

II. CMOS CURRENT REFERENCE

A. MOSFETs in Weak Inversion Region

A model of the proposed CMOS reference can be used to describe the working of an n-channel MOS transistor in the weak inversion region [15]. Under The characteristic of an n-channel MOS transistor operating in the weak inversion region is similar to that of a BJT transistor and can be described as

$$I_D = I_{D0} S e^{q(V_{GS}-V_{TH})/nkT} \quad (1)$$

where I_{DO} is the generation current, S is the geometrical shape factor of the transistor, q is the electron charge, n is a slope factor, k is the Boltzmann constant, T is the absolute temperature, V_{GS} is the gate-source voltage, and V_{th} is the threshold voltage of the transistor. From Eq. (1), the gate-source voltage of the MOSFET for a given drain current can be described as

$$V_{GS} = nV_T \ln\frac{I_D}{SI_D} + V_{TH} \quad (2)$$

where V_T is the thermal voltage which is equal to kT/q. In this equation, the threshold voltage of the MOSFET can be described as [15]

$$V_{TH} = -\frac{kT}{q}\ln\frac{N_{D,poly}}{N_A} + \frac{2\sqrt{kTN_A\varepsilon_{si}\ln\frac{N_A}{n_i}} - Q'_{SS}}{C'_{OX}} \quad (3)$$

where $N_{D,poly}$ is the doping concentration of donor atoms in the n+ poly gate and N_A is the doping concentration of acceptor atoms in the substrate, n_i is intrinsic carriers, ε_{si} is the relative dielectric constant of Silicon, Q'_{SS} is the surface-state charge, and $C'ox$ is the oxide capacitance per area.

Substituting Eq. (3) into Eq. (2) and taking the derivative of V_{GS} with respect to T, the temperature coefficient of V_{GS} can be written as

$$\frac{\partial V_{GS}}{\partial T} \approx n\frac{k}{q}\ln\frac{I_D}{SI_{D0}} - \frac{k}{q}\ln\frac{N_{D,poly}}{N_A} = -\frac{k}{q}\ln\frac{N_{D,poly}(SI_{D0})^n}{N_A(I_D)^n} \tag{4}$$

which indicates that the temperature coefficient of V_{GS} is a negative quantity.

B. Temperature Independent Current Reference

This section presents a temperature-compensated current reference, which is use an n-channel MOS transistor to operate in the weak inversion region [16]. In Fig.1, the circuit consists of a start-up circuit which is a PTAT current generator, a bandgap reference, and a zero-TC current replication circuit. The PTAT current generator generates a current proportional to absolute temperature, the value is given by

$$I_{PTAT} = \frac{nV_T}{R_1} ln\, K \tag{5}$$

where K is the size ratio of M_0 to M_1. The V_{ref} can be written as

$$V_{REF} = V_{GS,M9} + I_{PTC}R_2 \tag{6}$$

The gate-source voltage of M_9 and the voltage drop across R_1 can be reduced by an n-channel MOS transistor work in the weak inversion region. The voltage drop across R_2 can be increased by a positive current. Therefore, the temperature compensation of V_{ref} is finished and the I_{ZTC} can be written as

$$I_{ZTC} = \frac{V_{REF}}{R_2} \tag{7}$$

The current mirror comprising M_{11} and M_{12} copies I_{ZTC} to the output. The output reference current (I_{REF}) of the proposed current reference can be written as

$$I_{REF} = I_{ZTC}\frac{(W/L)_{12}}{(W/L)_{11}} = \frac{1}{R_2+R_3}(V_{GS,M9} + I_{PTAT}R_3)\frac{(W/L)_{12}}{(W/L)_{11}} \tag{8}$$

C. The opposite Characteristic curve Temperature Independent Current Reference

This section design a temperature-compensated current reference [17], which has the opposite characteristic curve comparing with the literature [16]. In particular, the standard current reference in Fig. 2 In this circuit the diode-connected nMOS transistor M5 has been added. The KVL of this circuit structure can be expressed as

$$V_{GS1} + V_{GS5} - V_{GS2} - mR_1 I = 0 \tag{9}$$

gives

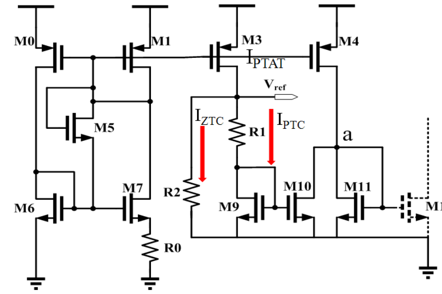

Fig. 1 Temperature compensation current reference

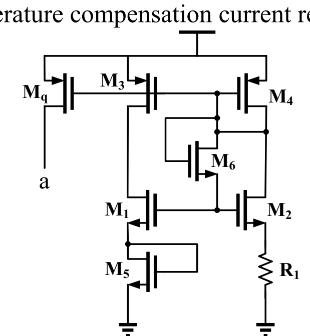

Fig. 2 The opposite characteristic curve temperature independent current reference

$$\sqrt{\frac{I}{\beta_{n0}}}\left(\frac{1}{\sqrt{\alpha_1}} + \frac{1}{\sqrt{\alpha_5}} - \sqrt{\frac{m}{\alpha_2}}\right) + V_{Tn} - mR_1 I = 0 \tag{10}$$

With reference to this circuit, the voltage drop across resistor R_1 is given by the sum of two terms with different temperature coefficients. One is related to the overdrive voltages of transistors M_2, M_3 and M_4 and has a positive temperature drift that is due to the negative drift of the mobility μ_n, while the other is the threshold voltage V_{Tn} whose temperature drift is related to different physical mechanisms [16]. Therefore, a reference current with a zero temperature coefficient can be obtained if the ratio and the size of these terms are properly chosen by design and temperature compensation is achievable. If the current ratio m is temperature independent, as in the standard MOS current mirror M_0-M_1, from Eq. 10, the temperature coefficient of the current can be expressed as

$$k_I = \frac{\left(2k_{VTn} + k_{u_n}\right)V_{Tn} - \left(2k_{R1} + k_{u_n}\right)mIR_1}{V_{Tn} + mIR_1} \tag{11}$$

On the basis of (11), if

$$\frac{k_{u_n} + 2k_{V_{Tn}}}{k_{u_n} + 2k_{R_1}} > 0 \tag{12}$$

k_I can be set to zero if

$$R_1 = \frac{V_{T_n}}{mI}\frac{k_{u_n} + 2k_{V_{Tn}}}{k_{u_n} + 2k_{R_1}} \tag{13}$$

In conclusion, temperature compensation can be achieved and the opposite characteristic curve current reference comparing with the literature[16] can be obtained. The proposed circuit combined Fig. 1 and Fig. 2 at point A to minimize the temperature variation.

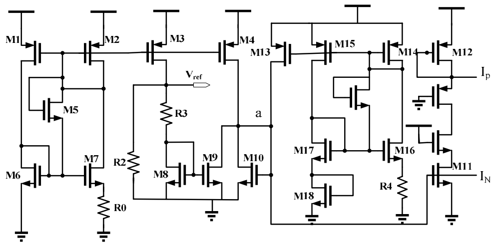

Fig. 3 Combination of the two architectures

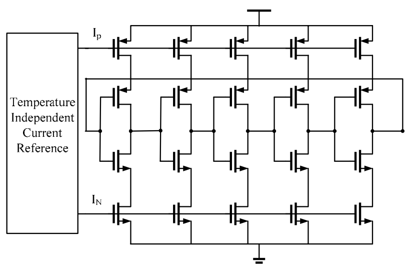

Fig. 4 Structure of CMOS ring oscillator with current-starved inverter stages

D. CURRENT CONTROLLED OSCILLATOR

The oscillation frequency of the ring oscillator, composed of N current-starved inverter stages, can be represented as[17]

$$f_{OSC} = \frac{1}{N \cdot \left(t_{PD\_rise} + t_{PD\_fall}\right)} = \frac{I_{source}}{N \cdot C_{load} \cdot V_{DD}} \tag{14}$$

Therefore, if I_{source} is stable with temperature drift, it can reduce the variation of oscillator's frequency obviously. Fig. 4 shows the structure of the ring oscillator, which is composed of an odd number of current-starved inverter stages with a temperature independent current reference.

III. SIMULATION RESULTS

The two kind of temperature-compensated current reference had been designed which have been presented in the previous Sections. The current references have been design -ed and simulated by HSPICE with reference to the models of the devices available in a 0.18 um CMOS technology.

The reference current versus temperature of temperature independent current reference is shown in Fig. 5 and the opposite characteristic curve current reference is shown in Fig. 6. It can be observed that the reference current, which has a nominal value of 1.315 uA at 25℃, has a residual temperature drift of about 0.96 nA in the temperature range between -25℃ and 75℃, in this range it shows a mean temperature drift of about 6.8 ppm/℃. In order to compensate the temperature drift of an oscillator itself, the temperature slope of proposed temperature independent current reference is slightly adjusted. The frequency of oscillator itself is proportional to temperature. Therefore the proposed current source is adjusted to complementary to temperature. Thus the currnet source is used to current controlled oscillator can achieve the oscillation frequency is 6.27 MHz and temperature drift of 14 kHz in range between -25℃ and 75℃. Based on this results, the temperature coefficients with the proposed oscillator is 22.3 ppm/℃. Thus the oscillation frequency has smaller temperature drift.

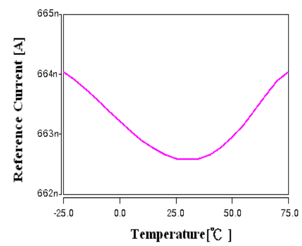

Fig. 5 Simulation plot of Fig. 1

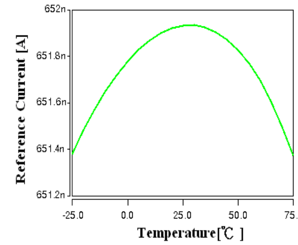

Fig. 6 Simulation plot of Fig.2

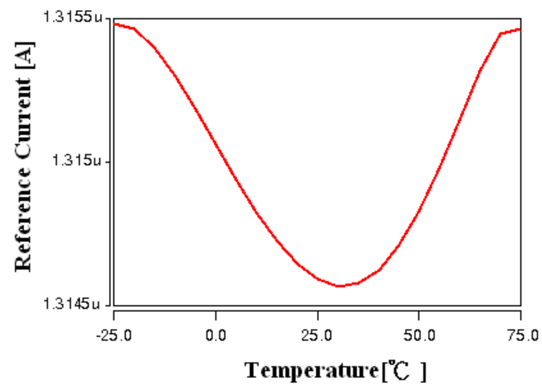

Fig. 7 Combination of the two architectures simulation plot

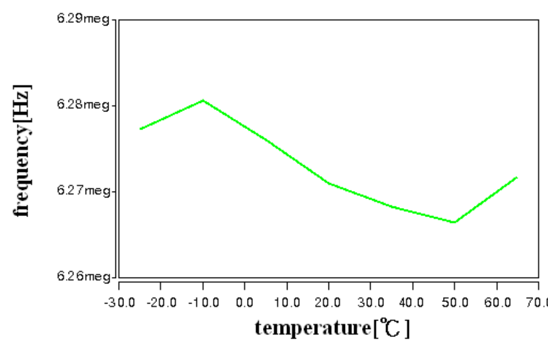

Fig. 8 The oscillation frequency versus temperature

IV. CONCLUSION

In this paper, the reference current source of combining two different temperature characteristic curve have been presented and analyzed. The temperature-compensated circuit, in particular, achieves a temperature drift of only 6.8 ppm/℃ in the temperature range between -25℃ and 75℃. The current controlled ring oscillator using this current source can oscillate to 6.27 MHz and the temperature coefficient 22.3 ppm/℃ is obtained. Both the current source and the current controlled ring oscillator have been designed by a 0.18 um CMOS technology process and their performances have been verified through computer simulations.

Acknowledgments

The authors would like to thank the National Chip Implementation Center and National Science Council, Taiwan, for fabricating this chip and supporting this work, respectively.

TABLE I
RING OSCILLATORS SPECIFICATION COMPARISON WITH REFERENCE

	Technology	Supply Voltage	Target Frequency	Temperature sensitivity	Power
This work	0.18 um	1.8 V	6.27 MHz	22.3 ppm/℃	32 uW
Y.-S. [18]	0.6 um	4 V	680 KHz	106 ppm/℃	0.4 mW
R. [19]	0.18 um	1.8 V	625 MHz	683 ppm/℃	0.59 mw
G. De [20]	0.35 um	1 V	80 KHz	824 ppm/℃	1.14 uW
K. R. [21]	0.13 um	3.3 V	1.25 GHz	340 ppm/℃	11 mW

V. References

[1] R. J. Widlar, "New developments in IC voltage regulators, " *IEEE J. Solid-State Circuits*, vol. SC-6, no. 1, pp. 2–7, Feb. 1971.

[2] K. E. Kuijk, "A precision reference voltage source," *IEEE J. Solid-State Circuits*, vol. SC-8, no. 3, pp. 222–226, Jun. 1973.

[3] A. P. Brokaw, "A simple three-terminal IC bandgap reference," *IEEE J. Solid-State Circuits*, vol. SC-9, no. 6, pp. 388–393, Dec. 1974.

[4] Y. P. Tsividis and R. W. Ulmer, "A CMOS voltage reference, " *IEEE J.Solid-State Circuits*, vol. SC-13, no. 6, pp. 774–778, Dec. 1978.

[5] R. W. Ye and Y. P. Tsividis, "Bandgap voltage reference sources in CMOS technology," *Electron. Lett.*, vol. 18, pp. 24–25, Jan. 1982

[6] E. Vittoz and J. Fellrath, "CMOS analog integrated circuits based on weak inversion operation," *IEEE J. Solid-State Circuits*, vol. SC-12, no. 3, pp. 224–231, Jun. 1977.

[7] C.-H. Lee and H.-J. Park, "All-CMOS temperature-independent current reference," *Electon. Lett.*, vol. 32, pp. 1280–1281, Jul. 1996.

[8] W. M. Sansen, F. Op't Eynde, and M. Steyaert, "A CMOS temperature compensated current reference," *IEEE J. Solid-State Circuits*, vol. 23, no. 3, pp. 821–824, Jun. 1988.

[9] J. Georgiou and C. Toumazou, "A resistorless low current reference circuit for implantable devices," in *Proc. IEEE Int. Symp. Circuits and Systems 2002. ISCAS 2002*, vol. 3, pp. III-193–III-196.

[10] O. Cerid, S. Balkir, and G. Dundar, "Novel CMOS reference current generator," *Int. J. Electron.*, vol. 78, pp. 1113–1118, Jun. 1995.

[11] I. M. Filanovsky and A. Allam, "Mutual compensation of mobility and threshold voltage temperature effects with applications in CMOS," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl*., vol. 48, no. 7, pp. 876–884, Jul. 2001.

[12] G. C. M. Meijer et al., "A new curvature corrected bandgap reference," *IEEE J. Solid-State Circuits*, vol. SC-17, no. 6, pp. 1139–1143, Dec.1982.

[13] B. Song and P. R. Gray, "A precision curvature-compensated CMOS bandgap reference," *IEEE J. Solid-State Circuits,* vol. SC-18, no. 6, pp. 634–643, Dec. 1983.

[14] M. Gunawan et al., "A curvature-corrected low-voltage bandgap reference,"*IEEE J. Solid-State Circuits*, vol. 28, no. 6, pp. 667–670, Jun.1993.

[15] R. J. Baker, "CMOS-Circuit Design, Layout and Simulation," 2nd ed., Piscataway, NJ: *IEEE Press,* 2005.

[16] Yoon-Suk Park; Hyoung-Rae Kim; Jae-Hyuk Oh; Yoon-Kyung Choi; Bai-Sun Kong;" Compact 0.7-V CMOS voltage current reference with 54/29-ppm/℃ temperature coefficient," *SoC Design Conference (ISOCC)*, Page(s): 496 – 499,2009

[17] Karim Arabi and Bozena Kaminska, "Built-In Temperature Sensors for On-Line Thermal Monitoring of Microelectronics Structures", IEEE International Conference on VLSI in computers and processors, pp. 462-467, 1997

[18] Y.-S. Shyu and J.-C. Wu, "A process and temperature compensated ring oscillator," in *Proc. 1st IEEE Asia Pacific Conf.*, 1999, pp. 283–286.

[19] R. Vijayaraghavan, S. K. Islam, M. R. Haider, and L. Zuo, "Wideband injection-locked frequency divider based on a process and temperature compensated ring oscillator, " *IET Circuits, Devices & Syst.*, vol. 3, pp. 259–267, 2009.

[20] G. De Vita, F. Marraccini, and G. Iannaccone, "Low-voltage low-power CMOS oscillator with low temperature and process sensitivity," in *Proc. IEEE Int. Symp. Circuits and Systems (ISCAS 2007),* 2007, pp. 2152–2155.

[21] K. R. Lakshmikumar, V. Mukundagiri, and S. L. J. Gierkink, "A process and temperature compensated two-stage ring oscillator, " in *Proc. IEEE Custom Integrated Circuits Conf. (CICC'07)*, 2007, pp. 691–694