Analysis and Design Considerations of Static CMOS Logics under Process, Voltage and Temperature Variation in 90nm CMOS Process

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***Abstract*—In this paper, we analyze the circuit characteristic of static CMOS logics and provide the size ratio of PMOS to NMOS transistors under process, voltage and temperature (PVT) variations in 90nm CMOS process. The threshold voltage of a MOS transistor is influenced seriously under PVT variations in ultralow voltages. The performances of the static CMOS logics are unstable under those conditions. To find the best size ratio region of PMOS to NMOS transistors, NOT, NAND, NOR, and XOR gates are simulated with various PVT conditions. Four kinds of gates are designed by different ratios respectively to compose the ring oscillators. By examining operating frequency, then we analyze the change of current according to various channel length and PVT conditions. By further analyzing the simulation results, if the channel length of MOS transistors is shorter than 200nm, or the operating voltage is lower than 0.5V, then the performance of MOS transistors is unstable in 90nm CMOS process. Through the data and the simulation provided by this paper, we can design the circuits with different needs, and we can also understand how each different section of PVT variations will affect the circuit in 90nm CMOS process.**

Keywords—90nm CMOS process; size ratio; Process-Voltage-Temperature (PVT) variations; ring oscillator; threshold voltage

I. INTRODUCTION

In 90nm CMOS process, there are too many abnormal performances when circuits operate at low voltage or sub-threshold voltage. In order to understand the causes, we especially did a study for how PVT variations will affect circuit performance [1]. After numerous simulation and analog, we collected a huge database and then use these data to do analysis and discussion. However, in many papers [2] often discussed about the PVT variations effects and the changing of the threshold voltage [3] and sub-threshold voltage [4,5] as process advances how to change MOS transistor's characteristics, these papers have been used as reference for the analysis of this paper, through these problems we simulate and analyze the results.

II. CHARACTERISTICS OF THE MOS TRANSISTOR

We know as the process advances, the size of the MOS transistor is made smaller and smaller. As device dimensions enter the generation of nanometer scale, there are a lot of problems in terms of device physics and process. Two of the biggest problems are short-channel effects and equivalent gate oxide thickness scaling (EOT). Among them, the greatest impact is made by the short-channel effects. However, there are still others effects such as channel carrier mobility and process variation.

A. Short-channel effects

The charges in space charge region from source and drain will extend into the channel at ideal channel length of MOS transistor with no bias voltage applied, but in contrast with the overall channel only occupy a small part of the whole. Essentially, all charges in the space charge region can also be controlled by voltage from gate. If the channel length become narrow, charges by gate voltage controlled will decline, charges in space charge region of drain will extend further into the channel, as shown as Fig. 1 [6], amount of charge numbers by gate controlled will decrease, so that threshold voltage roll-off, resulting in leakage current increases when components cut off, this effect make doping concentration in channel increase, and reduce the junction depth of source and drain while the gate dielectric layer thickness be lower [7]. In conclusion, the short-channel effects are attributed to two physical phenomena, the limitation imposed on electron drift characteristics in the channel and the modification of the threshold voltage due to the shortening channel length.

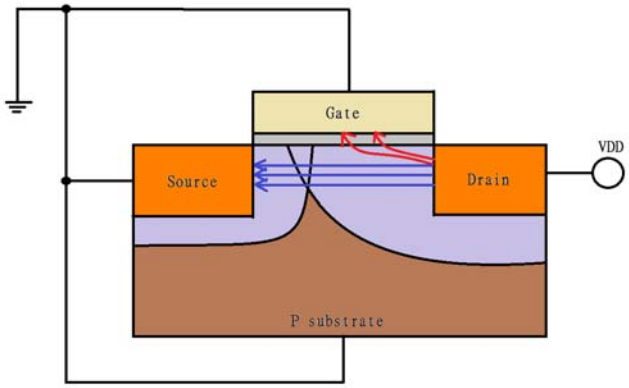

Fig. 1. Short-channel effects in Cross-section of a MOS transistor [6].

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III. ANALYSIS OF BASIC STATIC LOGIC GATES

In this experiment, we use four kinds of basic static logic circuits- NOT, NAND, NOR, XOR gates to do the analysis of this chapter. And we set the situation under 27 ˚C in process of TT region, set NOT gate and NOR gate's NMOS width at 200nm, and set NAND gate and XOR gate's NMOS width at 400nm. And we set MOS transistor's channel length at 100nm, 200nm, 300 nm, 400 nm, respectively. In order to reach the result in which the transitional voltage is just half of the operating voltage, we design the best MOS width of PMOS at various operating voltages (0.3V~1.0V) respectively, and then calculate the PMOS width over the NMOS width, we will get a trend curve about dimensional change when operating voltage is changing. So we can create an optimal dimensions database regardless of which operating voltage applied, and which channel length we set. In Fig. 3 we can find out that channel length plays an important role in the reason of different size ratio trend. Simulation in the upper left corner shows the result of size ratio while MOS transistor's channel length is set at 100nm and simulation in the upper right corner show the result of size ratio while MOS transistor's channel length is set at 200nm. Through these two simulations, we can conclude the variation of these different size ratios is caused by short channel effect. While PMOS width of the NOT gate is set at 450nm and we can get the result from Fig. 4. The threshold voltage of NOT gate's NMOS is changed because of the difference of sizes of channel length. The other side, in Fig. 5, we find out that the amount of changing threshold voltage decrease seriously when the channel length is shorter than 200nm. And we can explore relationships between changes of these two simulation graphs.

A. $|V_{thp}|/V_{thn}$ of the NOT gate while W_p=450nm

In Fig. 6, this simulation graph presents the threshold voltage of NOT gate's PMOS over threshold voltage of NOT gate's NMOS ($|V_{th}|$ of PMOS / V_{th} of NMOS). Obviously, the performance of channel length at 100 nm shown and the performance of channel length longer than 200 nm shown is completely different. And the channel length at 200 nm or longer, these trends of threshold voltage ratios are similar to each other. This analysis proves that short-channel effects change the characteristic of threshold voltage while the channel length is shorter than 200nm. And 450nm of PMOS width of NOT gate is the best size under 27 ˚C, process of TT region, 400nm of channel length, and 0.3V operating voltage supplied.

B. $|V_{thp}|/V_{thn}$ of the NOT gate while W_p=560nm

In order to prove that this phenomenon is not unique, we reset the PMOS width at 560nm, 560nm of PMOS of NOT gate is the best size under 27 ˚C, process of TT region, 100nm of channel length, and 1.0V of operating voltage supplied., in Fig. 7, we get this simulation result is similar to the above results, So we recommend that you set the channel length at 200nm or longer than 200nm, and the operating voltage to 0.5 volts or higher than 0.5V in 90nm CMOS process.

From another point, discussion on the W_P/W_N of NOT gate at different channel length, we can get the result in Fig. 8.

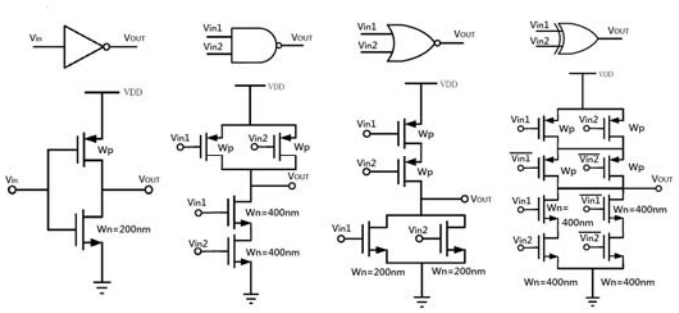

Fig. 2. Structures of NOT, NAND, NOR, XOR gates.

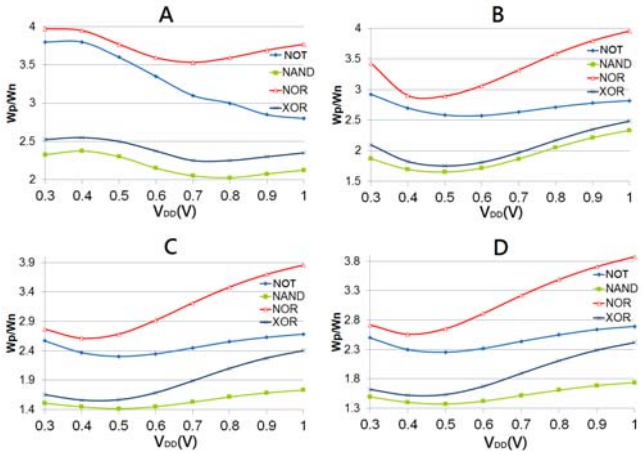

Fig. 3. Wp/Wn of NOT, NAND, NOR, XOR gate under various of VDD, (A) L=100nm. (B) L=200nm. (C) L=300nm. (D) L=400nm.

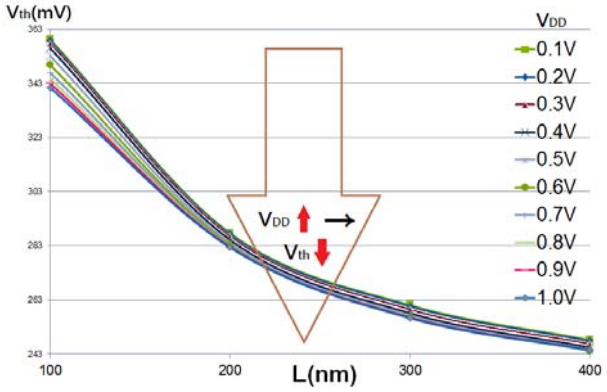

Fig. 4. The Vthn of NMOS of NOT gate.

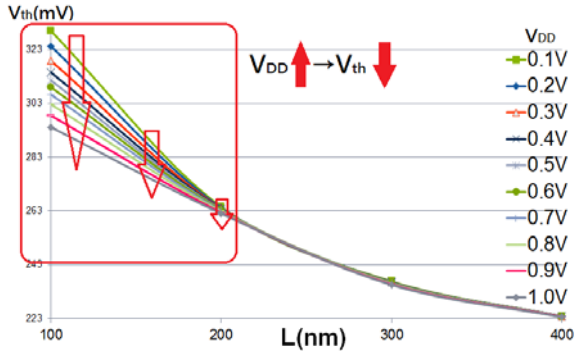

Fig. 5. The |Vthp| of PMOS of NOT gate.

IV. Analysis of Four Different Ring Oscillator Structures

As mentioned above, we use the static logic circuits with the best size ratio design in the process of TT region and under 27 ˚C, respectively. The four kinds of ring oscillator circuits are composed of NOT, NAND, NOR, XOR stages as Fig. 9 shown. Then we set the temperature at -40, 27, and 125 ˚C in process of SS, TT, and FF regions, and analyze the highest operating frequency of these circuits under a variety of operating voltage supply. After creating a huge database of the highest operating frequency with different PVT variations, we can explore the current changes with this database, because the operating frequency is positively related to the value of operating current. In Fig. 10.and Fig. 11, we get the result of maximum operating frequency and minimum operating frequency of each structure of ring oscillators. (The maximum operating frequency operated at 1.0V, in process of FF region, under -40 ˚C, and minimum frequency operated at 0.3V, in process of SS region, under -40 ˚C.)

A. *Analysis of the current and the maximum operating frequency*

In a general way, the current flowing through the MOS transistor will become smaller as the temperature get higher, but from the simulation graphs below, we see the exact opposite circumstance in low voltage operating region. In Fig. 12. , as operating voltage is lower than 0.6 volts, we find the temperature is higher, the higher the frequency of operation will be, representing the current will be higher with increasing temperature. As operating voltage is higher than 0.6 volts, we find it a normal phenomenon that the operating frequency and the current will become smaller with higher temperature. In Fig. 13. we can clearly see that when the ring oscillator's operating voltage is below a certain value, the operating frequency will increase with increasing temperature. Finally we can use this huge database analyze how PVT variations effects and different channel length will affect the characteristics of the MOS transistors, as the result in Table. 1.

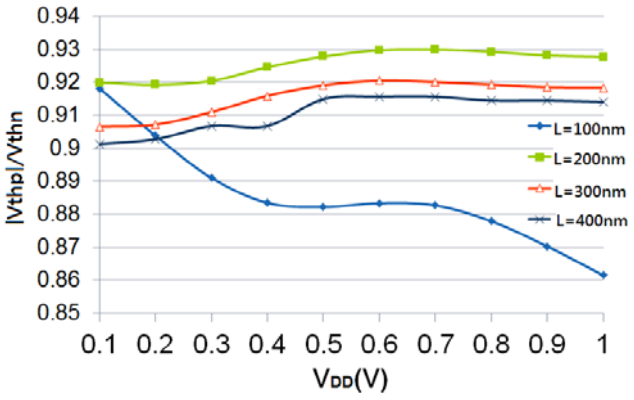

Fig. 6. $|V_{thp}|/V_{thn}$, W_p=450nm, L=100nm, 200nm, 300nm, and 400nm.

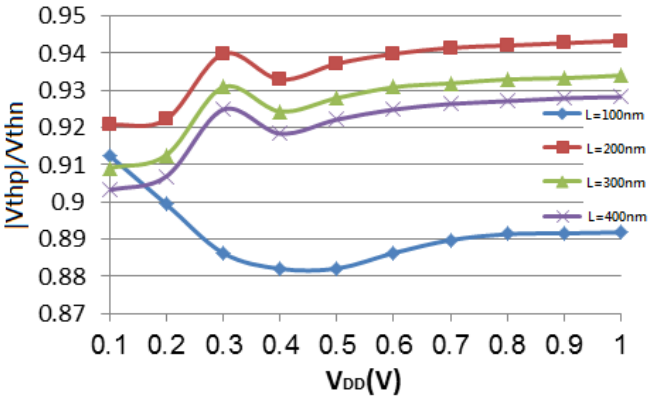

Fig. 7. $|V_{thp}|/V_{thn}$, W_p=560nm, L=100nm, 200nm, 300nm, and 400nm.

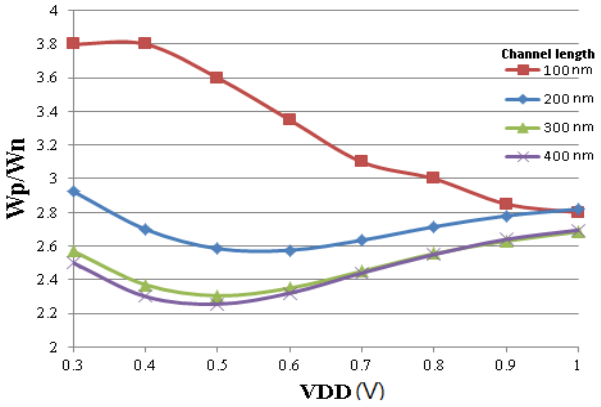

Fig. 8. Wp/Wn of NOT gate, L=100nm, 200nm, 300nm, and 400nm.

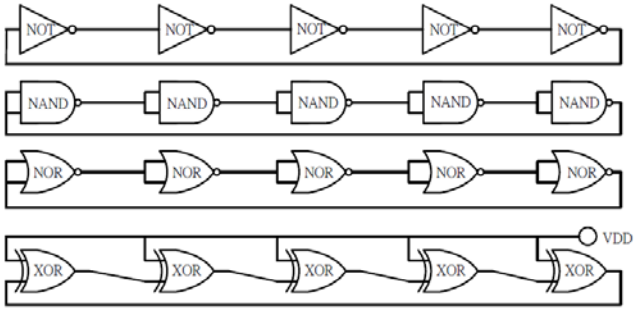

Fig. 9. Structure of the four kinds of ring oscillator.

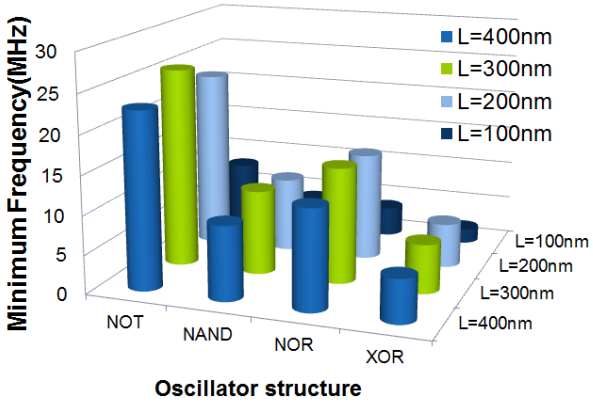

Fig. 10. Minimum frequency under SS, 0.3V, and -40˚C.

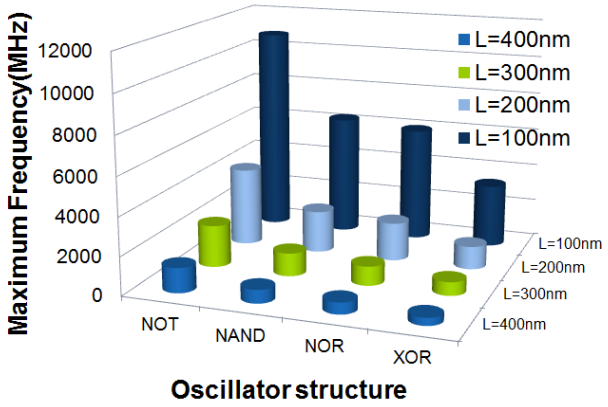

Fig. 11. Maximum frequency under FF, 1.0V, and -40˚C.

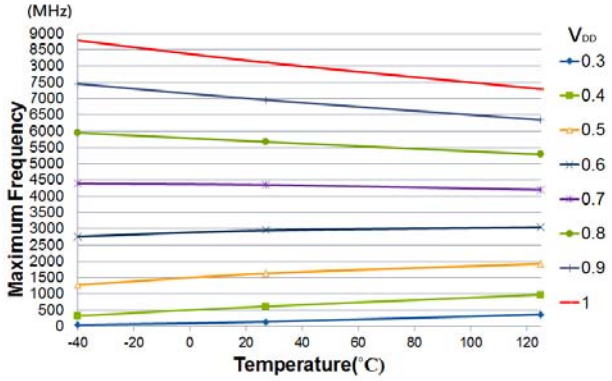

Fig. 12. Maximum frequency of oscillator of NOT gates under, TT, various operating voltage, various temperature.

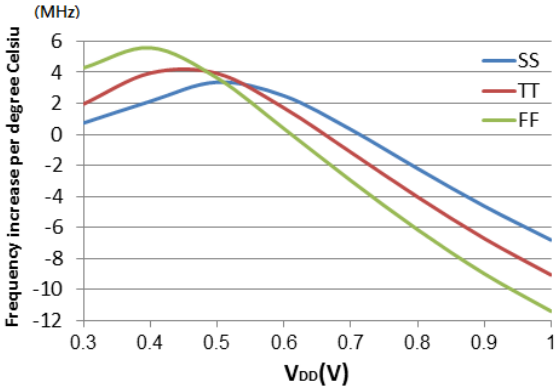

Fig. 13. Frequency increase/ ˚C of oscillator of NOT gates (channel length=100nm).

TABLE I. Characteristics of the MOS transistor with different operating voltage and channel length.

	Temp ↑	
	Freq ↑	Freq ↓
L=100nm	V_{DD} < 0.7V	V_{DD} > 0.7V
L=200nm	V_{DD} < 0.6V	V_{DD} > 0.6V
L=300nm	V_{DD} < 0.5V	V_{DD} > 0.5V
L=400nm	V_{DD} < 0.5V	V_{DD} > 0.5V

V. Conclusion

This paper presents the analysis of the circuit characteristic of static CMOS logics and provide the size ratio of PMOS to NMOS transistors under process, voltage and temperature (PVT) variations in 90nm CMOS process. Through this analysis we know the threshold voltage of a MOS transistor is influenced more seriously under PVT variations in ultralow voltages, and the performances of the static CMOS logics are really unstable under those conditions. In addition to designing the best size ratio for each logic circuit with various PVT conditions, we also discussed the performance of operating frequency of the ring oscillator. Followed by numerous simulations, we analyze the data and discuss the conclusions how PVT variables and channel length affect these circuits. Finally, we recommend that you try to select MOS transistor's channel length is longer than 200nm, and the operating voltage is supplied at 0.5 volts or higher, in order to avoid the unstable performance because PVT variable effects and channel length generated in the 90nm CMOS process. Conversely, we can use this abnormal performance on the device, the higher the temperature the greater the current of the circuit. Finally, we can also use the final simulation to design the device that current won't be changed as the temperature increase or decrease.

VI. Acknowledgement

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