Design of Low-Power Content Addressable Memory Cell

Content Addressable Memory (CAM), a large amount of energy is generally expended charging and discharging most of the match lines on most cycles. In this paper, a new low-power CAM cell design is proposed to reduce the comparison power of CAM cell. Moreover, in the CAM word circuit design, a staticpseudo nMOS logic structure with a precomputation approach is used to effectively avoid the frequently switching in the match lines. The HSPICE simulation results are based on TSMC 0.25 m μ CMOS process with2.5 V supply voltage. The power consumption of the proposed CAM is 16.38 mW under 300 MHz operation frequency. Moreover, the power-performance metric is13.33 fJ/bit/search for random inputs.