A 1.8-V 4-ppm/°C Reference Current with Process and Temperature Compensation

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Abstract

A current reference generator with a proposed compensation circuit against temperature variation is presented. The current reference generator provides a reference current of 10 uA with temperature coefficient (TC) of 4 ppm/°C under temperature range from -40 to 125°C. The circuit occupies 0.008 mm^2 in a 180-nm standard CMOS process.

Keywords: bandgap; temperature compensated; current reference; temperature coefficient;

1. Introduction

Present day the power and digital electronic of systems demand very stable, so the voltage or current references in the system are more important. The design of voltage references has requires low sensitivity to process, supply voltage and temperature variations, so bandgap references are usually have used.

The bandgap references demand large-area diodes or Bipolar Junction Transistors (BJTs) with 0.6V turn-on voltage at room temperature, and their power consumption is much larger[1],[2]. But now the product requirements must be low power consumption and low cost. For this purpose, many efforts have been made in research reliable voltage and current references in CMOS technology, and many high precision, temperature compensated reference circuits have been prop-osed in many literatures over the last decades[4]-[7]. Therefore subthreshold CMOS voltage references are has been published for that is reduce chip area and reach low supply requirements. However, the subthreshold CMOS references are usually very sensitive for process variation because of the threshold voltage (V_TH) variation[2],[8], and the reference voltage (V_REF) drifts up to 15% in the worst-case process variations[2],[9].

Usually a first order temperature compensation to achieve range inside 20 to 100 ppm/°C[10]-[12], in order to overcome such limitations limit, since there are many papers have proposed even more advanced method to solve the temperature compensation. As shown in Fig. 1 can know that this paper proposes circuit architecture. In this paper, proposes a method of second-order temperature compensated for circuit high performance in section II. The section III proposes the simulation of CMOS current reference assess the performance. And the conclusions are proposes in section IV.

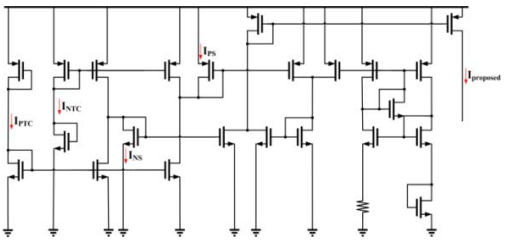

Fig. 1. Circuit architecture

2. Analysis architecture

MOSFETs in Subthreshold Region

A model of the standard CMOS reference that been used to describe the operating of an n-channel MOS transistor in the weak inversion region[13]. The behavior of an n-channel MOS transistor operating in the weak inversion region is similar to the behavior of BJT transistor and that can be described as

$$I_D = I_{D0} S e^{q(V_{GS}-V_{TH})/nkT} \quad (1)$$

where S is the geometrical shape factor of the transistor, I_{D0} is the generation current, k is the Boltzmann constant, T is the absolute temperature, q is the electron charge, n is a slope factor, V_{GS} is the gate-source voltage of the transistor, and V_{TH} is the threshold voltage of the transistor. From (1), the gate-

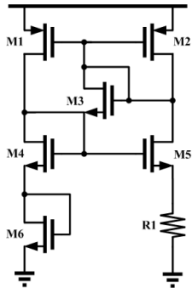

Fig. 2. The temperature compensated bias circuit

source voltage of the MOSFET for given drain current can be described as

$$V_{GS} = nV_T \ln\frac{I_D}{SI_D} + V_{TH} \tag{2}$$

where the thermal voltage of the transistor is V_T which is equal to kT/q. The threshold voltage of the MOSFET in (2) that can be described as

$$V_{TH} = -\frac{kT}{q}\ln\frac{N_{D,poly}}{N_A} + \frac{2\sqrt{kTN_A\varepsilon_{si}\ln\frac{N_A}{n_i}}-Q'_{SS}}{C'_{OX}} \tag{3}$$

where N_A is the doping concentration of acceptor atoms in the substrate, $N_{D,poly}$ is the doping concentration of donor atoms in the n+ poly gate, C'_{OX} is the oxide capacitance per area, ε_{si} is the relative dielectric constant of Silicon, n_i is intrinsic carriers, and Q'_{SS} is the surface-state charge. Substituting (3) into (2) and taking the derivative of V_{GS} to T to do differential, so the TC of V_{GS} can be written as

$$\frac{\partial V_{GS}}{\partial T} \approx n\frac{k}{q}\ln\frac{I_D}{SI_{D0}} - \frac{k}{q}\ln\frac{N_{D,poly}}{N_A}$$

$$= -\frac{k}{q}\ln\frac{N_{D,poly}(SI_{D0})^n}{N_A(I_D)^n} \tag{4}$$

which proves that the TC of V_{GS} is the negative quantity.

Temperature Independent Current Reference

This section which designs a temperature compensated current reference [14]. In particular, this circuit which the diode-connected NMOS transistor M6 has been added of the standard current reference circuit in Fig. 2. The KVL of this circuit structure that can be expressed as

$$V_{GS4} + V_{GS6} - V_{GS5} + mR_1I = 0 \tag{5}$$

,and gives

$$\sqrt{\frac{1}{\beta_{n0}}}\left(\frac{1}{\sqrt{\alpha_4}} + \frac{1}{\sqrt{\alpha_6}} - \sqrt{\frac{m}{\alpha_5}}\right) + V_{TH} - mR_1I = 0 \tag{6}$$

To reference to this circuit, the drop voltage across the resistor R_1 is given by the sum of two items with different temperature coefficients. One is about for the

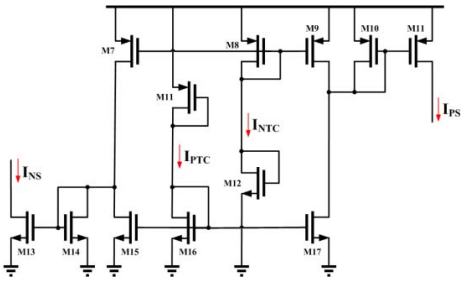

Fig. 3. Compesnated temperature coefficient circuit

overdrive voltages of transistors M1, M2 and M5 and those has a positive temperature drift that is because of the negative drift of the mobility μn affect, the other is the threshold voltage VTH which temperature drift is due to different physical mechanisms [15]. Therefore, if the ratio and the size of these items could be properly chosen by design and temperature compensation is achievable that the reference current with a zero-TC could be obtained. From (6), as in the standard MOS current mirror M1-M2, when the current ratio m is temperature independent, the TC of the current can be expressed as

$$k_I = \frac{(2k_{V_{TH}}+k_{\mu_n})V_{TH}-(2k_{R_1}+k_{\mu_n})mIR_1}{V_{TH}+mIR_1} \tag{7}$$

From the basis of (7), if

$$\frac{k_{\mu_n}+2k_{V_{TH}}}{k_{\mu_n}+2k_{R_1}} > 0 \tag{8}$$

k_I can be set to zero, if

$$R_1 = \frac{V_{TH}}{mI}\frac{k_{\mu_n}+2k_{V_{TH}}}{k_{\mu_n}+2k_{R_1}} \tag{9}$$

In conclusion, temperature compensation can be achieved and the opposite characteristic curve current reference comparing with the literature[15] can be obtained.

Compensated and optimized temperature coefficient

This section presents with compensation and optimized TC circuit, which used two the different TC of currents to generate a current is generated at any temperature. As shown in Fig. 3, begin, generate two different TC currents that one is positive temperature coefficient of current (I_{PTC}) by M11 to generated, and the other is negative temperature coefficient of current (I_{NTC}) by M12 to generated. Second, use the I_{PTC} that from M16 mirror to M17 minus the I_{NTC} that from M8 mirror to M9. Accordance with above as shown, we can get the current that from M10 mirror to M11 which generated current is defined positive slope of current (I_{PS}) that can tuned the I_{PTC} value to decide the final

TABLE I. COMPARISON OF CURRENT REFERENCE PERFORMANCES

	Technology (μm)	Supply Voltage(V)	Target Current(μA)	Temperature Range(°C)	Temperature Coefficient(ppm/°C)
TCASII,2005[7]	0.35	2.5	13.65	-30 to 100	28
ASSC,2009[16]	0.35	3.3	17	-20 to 100	280
TCASI,2007[17]	0.18	1	144	0 to 100	185
JSSC,2012[18]	0.18	1	7.81	0 to 100	24.9
This Work	0.18	1.8	10	-40 to 125	4

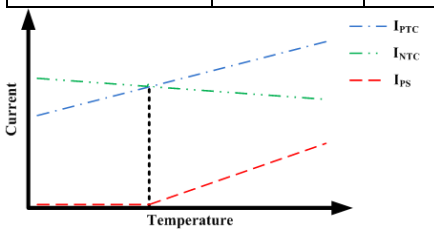

Fig. 4. Positive slope of current

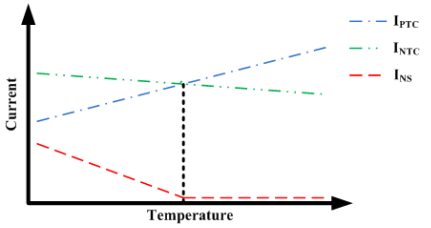

Fig. 5. Negative slope of current

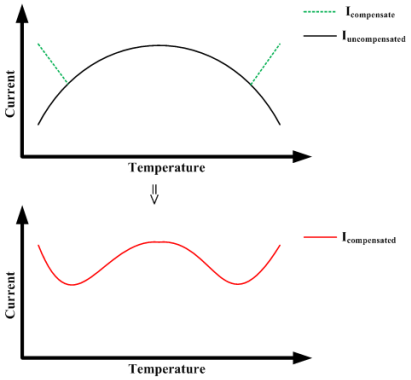

Fig. 6. Reference current has been compensated

current at which temperature began to rise. And if the I_{NTC} that from M8 mirror to M7 minus the I_{PTC} that from M16 mirror to M15, we can get the current that from M14 mirror to M13 which generated current is defined negative slope of current (I_{NS}) that also can tuned the I_{NTC} value to decide the final current decreased to which temperature.

However, throw the Fig. 4 and Fig. 5 to compensate the uncompensated of current that shown as Fig. 6. From Fig. 6 can know that because of the left arc could be raised, and the right arc also could be raised, the uncompensated temperature current of maximum current temperature drift is smaller than the compensated temperature current of maximum current. Then the temperature coefficient of the compensated current is the smaller than the temperature coefficient of uncompensated current. Thus learned the circuit architecture can get better TC compensation.

3. Simulation results

This circuit has been designed and simulation by SPECTRE with reference modes of devices available in 180 nm CMOS technology. The target temperature independent of current is 10uA and that the simulation temperature environments range from -40 to 125°C, and supply voltage is 1.8 V.

As shown in Fig. 7, from bias circuit generates the current that max current drift of temperature is 52 nA, and it is mean the TC is 41.6 ppm/°C. Fig. 8 is show the second-order temperature compensated circuit generates currents, one is from 50 to 125°C has the I_{PTC}, and the other is from -40 to 60°C has the I_{NTC}. When the current of bias circuit add the currents of the compensated circuit, the current of bias circuit can get the I_{PTC} from 50 to 125°C compensated and the I_{NTC} from -40 to 60°C compensated. Then it could obtain the current after compensated that shown in Fig. 9. From the Fig. 9, the compensated current that max current drift of temperature is 5 nA, and it is mean the TC is 4 ppm/°C.

However, let the uncompensated TC of current compared with the compensated TC of current can know that the compensated TC of current is ten times better than the uncompensated TC of current. Thus the simulation results shown can know this architecture Fig. 1 that can obtained the great TC compensated. Shown as Table I., that can see the comparison of reference current performances with other literature.

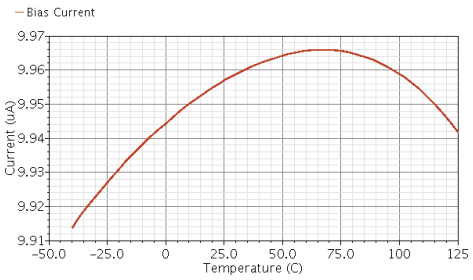

Fig. 7. Bias current without compensated

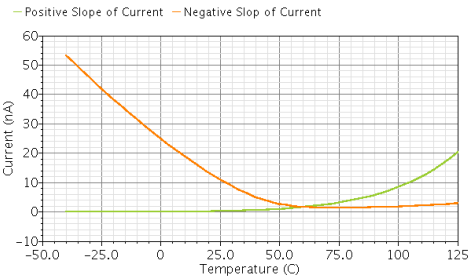

Fig. 8. Compensation current

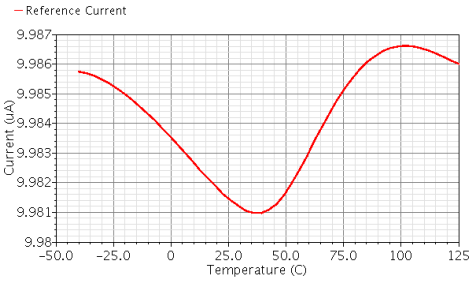

Fig. 9. Target current with compensated

4. Conclusions

In this paper, temperature compensation circuit can be adjusted current at any temperature rise that can be achieved to make compensation for the effect of the target current value. The proposed circuit has been implemented in a 0.18-um standard CMOS process and the supply voltage of 1.8V. The target current is 10uA that achieved the small TC of 4 ppm/°C with temperature range from -40 to 125°C, which has a high effect for the temperature variation calibrate. While feasibility of the proposed concept has been shown, this circuit architecture has many parts that need improvement in the future.

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