A GHz Full-Division-Range Programmable Divider with Output Duty-Cycle Improved

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***Abstract*—This work presents a full-division-range programmable frequency divider with a 50% duty-cycle output. The proposed programmable frequency divider includes a programmable counter (PC) and duty-cycle improved circuit (DCIC) to achieve a full-division-range, low-area, and close-to-50% duty-cycle output from an input clock with an arbitrary duty cycle. A chip was fabricated using a 0.18-µm standard CMOS process with a 1.8-V power supply. The measurement results show that the proposed programmable frequency divider can operate from 1 MHz to 1 GHz, and the division ratio ranges from 1 to 63. When the input divisor is 20, the input clock is 700 MHz, the input duty-cycle is 20%, and output duty-cycle is 50.4%. The total power consumption of the proposed programmable frequency divider is only 0.62 mW at 700 MHz, and the active die area is only 0.125 × 0.05 mm^2.**

Keywords—duty cycle; full-division-range; programmable frequency divider

I. INTRODUCTION

In the past, most conventional frequency dividers were used in phase-locked loops (PLLs) to generate a high-frequency output clock from a stable low-frequency external signal [1], [2]. However, because the system complexity and clock variants have increased significantly in recent years, a programmable frequency divider has become crucial for various applications [3]. These applications can generally be identified by their need for 50% duty-cycle input clocks, such as (1) switched capacitor-based circuits (SCC), taking the pipelined analog-to-digital converter (ADC) for example, inputting the 50% duty-cycle clock would ensure each stage of pipelined ADC to have an same amount of time to settle [4]; (2) DRAM, which doubles the data transfer rate using the rising and falling edge of a 50% duty-cycle clock input [5]; (3) low-power (LP) systems, where the dynamic frequency scaling (DFS) technique is employed to enable the system to adopt a low-power consumption mode by altering the operating frequency using a programmable frequency divider [6]; and (4) other circuits, where the various 50% duty-cycle input frequencies have been provided to different circuits by altering the division of the divider [7], as shown in Fig. 1. Therefore, a full division ratio and low-area programmable frequency divider with a 50% duty-cycle output is extremely useful for these applications. However, although previous programmable frequency dividers [1], [2], [8], [9] and [10] provide wide division ratios, they do not produce 50% duty-cycle output clocks, limiting their value for the above applications. Additionally, the narrow pulse width is sensitive to process, voltage, temperature, and loading (PVTL) variations, causing incorrect operations and reducing system robustness. Therefore, several programmable frequency dividers [3], [11] have been presented to improve the output duty-cycle. However, although a wider range of input divisors is available for these programmable frequency dividers, they still cannot achieve a full-range division.

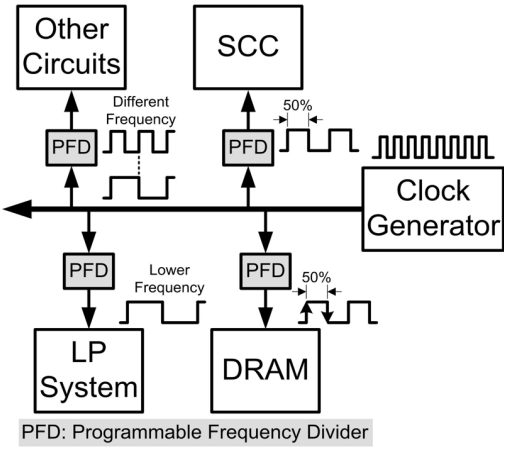

Fig. 1. Applications of the programmable frequency divider with an improved duty-cycle output.

This work presents a programmable frequency divider that can achieve a full-range division and improve the output duty-cycle to 50%. The proposed programmable frequency divider has four key advantages: (1) the reload generator and duty reload generator are simple and can be easily extended for higher division ranges; (2) a continuous and full-range divisor can be achieved from 1 to 2^n-1; (3) the duty-cycle output pulse width is approximately 50% and varies by less than 0.7% for various input divisors; and (4) the core area is extremely small.

II. PROPOSED PROGRAMMABLE FREQUENCY DIVIDER

A. Proposed Architecture and Operation Principle

Fig. 2 shows the proposed programmable frequency divider, which comprises a programmable counter (PC) and

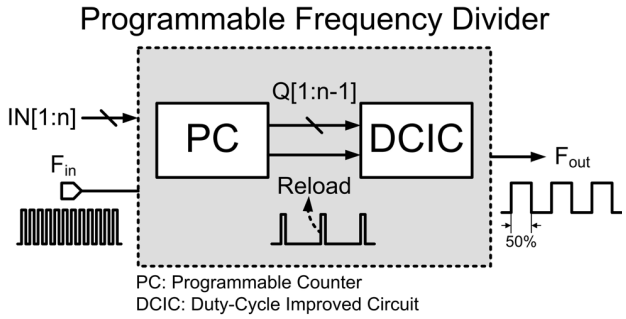

Fig. 2. Proposed programmable frequency divider.

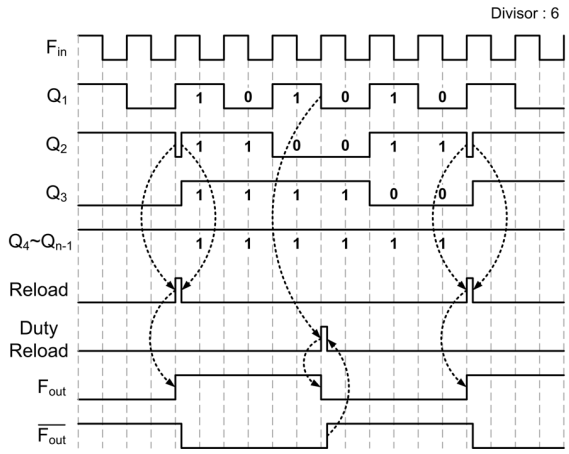

Fig. 3. Timing diagram of the proposed programmable frequency divider.

duty-cycle improved circuit (DCIC).The signal F_{in} is the input clock and the signal IN[1:n] is the input binary divisor. The internal signal Q[1:n-1] is the binary counting result from the PC, and the signal Reload is the output of the PC. Additionally, the signal reloads the full divider. The signal F_{out} is the output clock of the programmable frequency divider. To explain the operation principle, a timing diagram of the programmable frequency divider when the input divisor is 6 is shown in Fig. 3. When the input clock F_{in} is activated, the PC begins counting and simultaneously sends a result signal Q[1:n-1] to the DCIC. When the PC counts down to the complement of input divisor IN[1:n], the PC generates a reload signal to reload the programmable frequency divider. The signal Reload is also sent to the DCIC, charging the output clock F_{out} to high. Then, because the reloading is already accomplished, the PC discharges the signal Reload to low. Subsequently, the DCIC generates an internal signal Duty Reload to discharge the output clock F_{out} to low as the PC counts down to suitable results. Here, the complement output $\overline{F_{out}}$ is charged to high, which discharges the signal Duty Reload signal to low using the DCIC. Finally, a period of output is generated, providing an output frequency that is one-sixth of the input clock and 50% of the output duty-cycle.

B. Programmable Counter (PC)

To achieve full-division-range feature as compared to that of a conventional programmable frequency divider [12], the

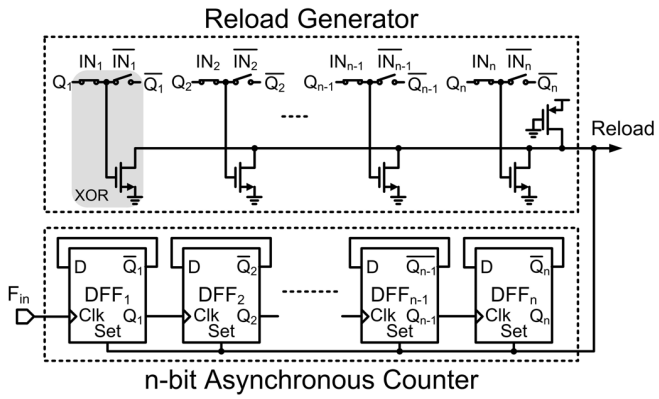

Fig. 4. Proposed programmable counter.

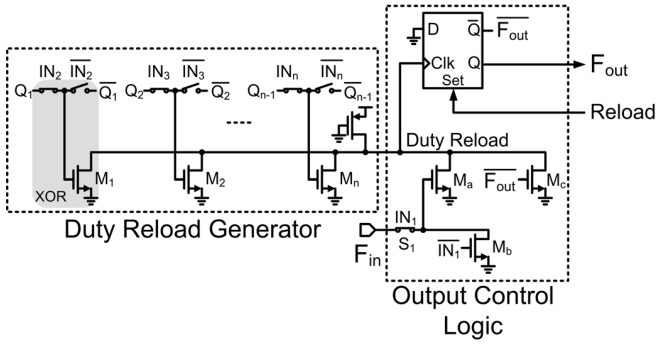

Fig. 5. Proposed duty-cycle improved circuit.

proposed PC includes an n-bit asynchronous counter and a reload generator, as shown in Fig. 4. In the asynchronous counter, the signal $\overline{Q_n}$ is connected to input node D form a divide-by-two stage in every D flip-flop. Therefore, n divide-by-two stages form an n-bit asynchronous counter, where the Q[1:n] is the binary counting result. Generally, the asynchronous counter counts down from 2^n-1 and generates result Q[1:n] to control the reload generator simultaneously. The reload generator comprises 2n transmission gates as switches, n NMOS transistors, and a turned-on PMOS transistor as the pseudo-NMOS logic. Every two transmission gates and one NMOS transistor form a XOR gate. When the Q_n and IN_n signals differ at the signal level, the NMOS transistor turns off and the turned-on PMOS transistor charges the signal Reload to high. Thus, all the NMOS transistors of the reload generator are turned off and the signal Reload will reloads the asynchronous counter when the asynchronous counter counts to the complement of IN[1:n]. Then, the NMOS transistor discharges the signal Reload to low and the frequency divider operation is complete.

The proposed PC not only maintains the full-range division, but also adopts a low-area design and can be easily extended to higher division ranges using the simplify reload generator. Only a D flip-flop, two transmission gates, and a NMOS transistor are required to add one bit. Furthermore, because the input clock F_{in} is connected to the D flip-flop, which is triggered by the rising edge, the output duty-cycle is not affected by the input regardless of the input duty-cycle. However, the reload signal of the proposed PC provides a

narrow output duty-cycle because the output clock has a high level only when the reload generator reloads the asynchronous counter. Fortunately, this disadvantage can be avoided by using a duty-cycle corrector (DCC) [5]. In this work, a duty-cycle improved circuit (DCIC) that is based on the concept of proposed PC has been presented to improve the output duty-cycle to 50%.

C. Duty-Cycle Improved Circuit (DCIC)

The proposed DCIC comprises a duty reload generator, which is similar to a reload generator, and output control logic, as shown in Fig. 5. The duty reload generator also uses a transmission gate and NMOS transistor to form n-1 XOR gates. The output control logic comprises a D flip-flop, a switch S_1, and three NMOS transistors. The key characteristic of this circuit is that the binary shifting caused by the binary code shifting slightly to the right is the same as altering the value by half. For example, assume the input divisor is 32, the binary code of 32 is $(\underline{1}00000)_2$ and the half value of 32 is 16. The binary code of 16 is $(0\underline{1}0000)_2$, which is the same as when a binary code of 32 shifts slightly to the right for one bit. Thus, the signal IN[2:n] of the duty reload generator is shifted right a XOR gate to alter the input divisor to half its original value, as shown in Fig. 5. However, binary shifting cannot provide accurate changes when the input divisor is an odd number. Therefore, two NMOS transistors M_a and M_b and a switch S_1 are included in the output control logic to assess the input divisor. When the PC counts to the correct results, all the NMOS transistors M_1 to M_n of the duty reload generator are turned off and the output control logic enters the judging mode. Because whether the input divisor is an odd or even number is decided by the least significant bit (LSB), IN_1, when the signal IN_1 is high, the input divisor is odd, causing switch S_1 to close and the NMOS transistor M_a waiting for the input clock F_{in} to become low. When the F_{in} is low, the NMOS transistor M_a turns off and the turned-on PMOS transistor charges the signal Duty Reload to high. When the signal IN_1 is low, the input divisor is even, causing switch S_1 to open and the NMOS transistor M_a to be turned off by the NMOS transistor M_b. Then, the turned-on PMOS transistor charges the signal Duty Reload to high immediately. After the assessment, the output control logic improves the output duty-cycle to 50% using the signals Reload, Duty Reload, and a D flip-flop. When the signal Reload is high, setting D flip-flop causes the output clock F_{out} to charges to high; whereas when the signal Duty Reload is high, the output clock F_{out} becomes low. Meanwhile, setting $\overline{F_{out}}$ to high discharges the signal Duty Reload to low using the NMOS transistor M_c. This technique is similar to that of conventional DCCs, which improve the output duty-cycle using rising and falling signals. The simple topology and logic of DCIC not only corrects the duty-cycle output pulse width to approximately 50%, but also provides a low-area design that can be low area and easily extended to higher divisor ranges.

III. EXPERIMENTAL RESULTS

The proposed programmable frequency divider was fabricated using a 0.18-μm standard CMOS process with a supply voltage of 1.8. The die photo of the proposed programmable frequency divider is shown in Fig. 6, and the

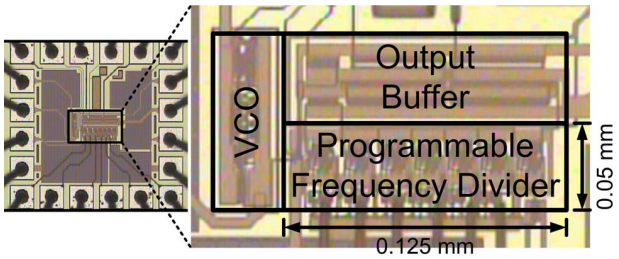

Fig. 6. Die photo of the proposed programmable frequency divider.

Fig. 7. Output waveforms of the proposed programmable frequency divider when Fin is 800MHz and the input divisor is 63.

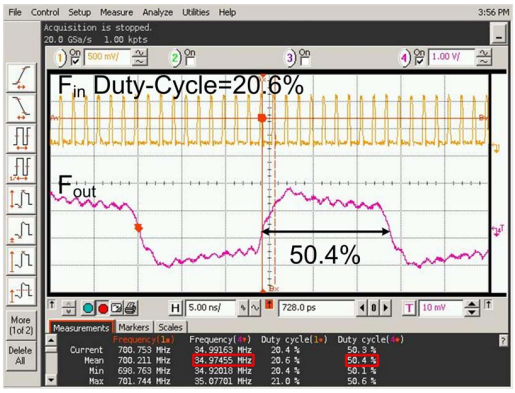

Fig. 8. Output waveforms of the proposed programmable frequency divider when Fin is 700MHz, the input divisor is 20, and the input duty-cycle is 20%.

active area was 0.125 × 0.05 mm^2. To compare the performance of the proposed programmable frequency divider with that of previous works, a six-stage counter was achieved in the chip. To verify the proposed programmable frequency divider, a voltage-controlled oscillator (VCO) is also fabricated. Fig. 7 shows the output waveforms of the proposed programmable frequency divider when the input divisor is 63 and the F_{in} is 800 MHz. The output waveforms show that the output frequency of the proposed programmable frequency divider is accurate when the input frequency varies. Additionally, the measured mean value of the output duty-cycle for the proposed programmable frequency divider at 800 MHz was 49.9%, achieving the desired 50% duty-cycle output. Fig. 8 shows the output waveforms of the proposed programmable frequency divider when the input divisor is 20,

TABLE I. COMPARISON WITH THE RESULTS OF PREVIOUS WORKS

	[1]	[3]	[8]	[10]	[11]	This Work
Architecture	PFD	PFD with DCC	PFD	PFD	PFD with DCC	PFD with DCC
Technology (μm)	0.18	0.18	0.18	0.18	0.18	0.18
Supply Voltage (V)	1.5	1.8	1.5	1.8	1.8	1.8
Input Clock (MHz)	~3500	~2500	~3000	~1800	0.1~2500	1~1000
Output Duty-Cycle (%)	N/A	44.4~50	N/A	N/A	33~66	50~50.7 @ 700 MHz
Division Range	13~1278	8~510	13~1278	N/A	8~1023	1~63
Core Area (mm^2)	0.04	0.1	0.04	0.011	0.04	0.00625
Power (mW)	3.23 @3.5 GHz	15 @ 2.5 GHz	3.58 @ 3 GHz	5.8 @1.8 GHz	12 @ 2.5 GHz	0.62 @ 0.7 GHz
FOM (GHz/mW)	1.08	0.17	0.84	0.31	0.21	1.13

PFD: Programmable frequency divider DCC: Duty-cycle correction

the F_{in} is 700 MHz, and input duty-cycle is 20.6%. The output waveforms show that the proposed programmable frequency divider not only can operate correctly at 700 MHz, but it also improves the narrow duty-cycle input to 50% duty-cycle output.

Table I shows a comparison between the results of several previous works and the proposed programmable frequency divider using the same CMOS technologies. The figure of merit (FOM) used to compare the results was defined as the operation frequency of the circuit for each milliwatt of power consumption (GHz/mW). Results indicate that the proposed frequency divider provides the lowest core area, lowest power consumption, and highest FOM using a simple architecture. The power consumption and FOM of the proposed divider were only 0.62 mW and 1.13, respectively. Compared with [3] and [11], this work provides a more accurate 50% duty-cycle output. Additionally, although the divisor range is smaller than that of previous works, it can be easily extended to higher divisor ranges. For example, if a 10-bit asynchronous counter is employed, the divisor range can be extended from 1 to 1023, realizing the design of full-division-range and low-area programmable frequency divider with a 50% duty-cycle output.

IV. CONCLUSION

This work proposed a full-division-range low-area programmable frequency divider with a 50% duty-cycle output. The proposed PC not only provides the full input divisor range, but it also adopts a low-area design and can be easily extended to higher divisor ranges using simplified architecture. Additionally, the proposed DCIC improves the duty-cycle output pulse width to 50%. The measurement results show that the proposed programmable frequency divider has a full division ratio ranging from 1 to 63, close-to-50% output duty-cycle and a low-power consumption of only 0.62 mW at 700 MHz. Moreover, the core area of the proposed programmable frequency divider is only 0.125×0.05 mm^2. Therefore, the proposed divider is suitable for applications that require varied frequencies and accurate 50% duty-cycle inputs.

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REFERENCES

[1] K. Y. Kim, Y. J. Min, S. W. Kim, and J. Park, "Low-Power Programmable Divider with a Shared Counter for Frequency Synthesizer," *IET Circuits Devices Systems*, vol. 5, no. 3, pp. 170–176, May. 2011.

[2] C. S. Lin, T. H. Chien, and C. L. Wey, "A 5.5-GHz 1-mW Full-Modular-Range Programmable Frequency Divider in 90-nm CMOS Process," *IEEE Trans. on Circuits and Syst. II: Express Briefs*, vol. 58, no. 99, pp. 550–554, Sept. 2011.

[3] M. Zhang, S. K. Islam, and M. R. Haider, "Efficient Driving-Capability Programmable Frequency Divider with A Wide Division Ratio Range," *IET Circuits Devices Systems*, vol. 1, no. 6, pp. 485–493, Dec. 2007.

[4] S. Karthikeyan, "Clock Duty Cycle Adjuster Circuit for Switched Capacitor Circuits," *IEEE Electronics Letters*, vol. 38, no. 18, pp. 1008–1009, Aug. 2002.

[5] T. H. Lin, C. C. Chi, W. H. Chiu, and Y. H. Huang, "A Synchronous 50% Duty-Cycle Clock Generator in 0.35μm," *IEEE Trans. on Very Large Scale Integration (VLSI) Syst.*, vol. 19, no. 4, pp. 585–591, Apr. 2011.

[6] G. M. Almeida, R. Busseuil, E. A. Carara, N. Hébert, S. Varyani, G. Sassatelli, P. Benoit, L. Torres, and F. G. Moraes, "Predictive Dynamic Frequency Scaling for Multi-Processor Systems-on-Chip," *IEEE Int. Symposium on Circuits and Syst. (ISCAS)*, pp. 1500–1503, May. 2011.

[7] H. Omran, K. Sharaf, and M. Ibrahim, "A Low-Power Digital Frequency Divider for System-on-a-Chip Applications,"*IEEE Int. Midwest Symposium on Circuits and Syst.*, pp. 1–4, Aug. 2011.

[8] K. Y. Kim, W. K. Lee, H. Kim, and S. W. Kim, "Low-Power Programmable Divider for Multi Standard Frequency Synthesizers Using Reset and Modulus Signal Generator," *IEEE Asian Solid-State Circuits Conf.*, pp.77–80, Nov. 2008.

[9] T. Khan, and K. Raahemifar, "An Ultra-Low Power 200MHz-1GHz Programmable Frequency Divider with Novel Clear/Preset D-Latch," *IEEE Int. Midwest Symposium on Circuit and Syst.*, pp. 985–988, Aug. 2010.

[10] X. P. Yu, M. A. Do, L. Jia, J. G. Ma, and K. S. Yeo, "Design of a Low Power Wide-Band High Resolution Programmable Frequency Divider," *IEEE Trans on Very Large Scale Integration (VLSI) Syst.*, vol. 13, no. 9, pp. 1098–1103. Sept. 2005.

[11] S. Wang, J. Wu, M. Zhang, F. Huang, L. Tang, and X. Ji, "A Wide Division-Ratio Range Programmable Frequency Divider with Driving-Capability Improved," *Analog Integrated Circuits and Signal Processing*, vol. 63, no. 3, pp. 509–514, Mar. 2010.

[12] S. H. Lee, and H. J. Park, "A CMOS High-Speed Wide-Range Programmable Counter," *IEEE Trans. on Circuits and Syst. II: Analog and Digital Signal Processing*, vol. 49, no. 9, pp. 638–642, Sept. 2002.