# A 400 MHz 500-fs-Jitter Open-Loop DLL-Based Multi-Phase Clock Generator Utilizing an Noise-Free All-Digital Locking Detection Circuitry

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***Abstract*—An open-loop DLL-based multi-phase clock generator for low jitter applications is designed in 0.13μm CMOS technology. A noise-free all-digital locking detection circuitry (AD-LDC) is designed to detect whether the DLL is locked in time domain. Besides, a current-mismatch free, supply-regulated charge pump is also proposed. As the DLL operating in the open-loop mode, an rms jitter of 500 fs is achieved at the frequency of 400 MHz. The entire circuit occupies 0.01 mm$^2$ and consumes 14 mW. The low jitter multi-phase clock generator can be applied for high-speed ADCs/DACs and wire line transceivers.**

## I. INTRODUCTION

Multiplying delay-locked loops (MDLLs) are attractive recently due to its better jitter performance as compared to that of phase-locked loops (PLLs) [1-4]. But in MDLLs, strong reference spurs appear at output of the MDLLs owing to periodic insertion of the clean reference clock. In DLLs, jitter comes from phase noise which is mainly contributed by a phase-frequency detector (PFD), mismatch of a charge pump (CP) and delay cells. To have better jitter performance, PFD and CP could be turned off after the DLL has been locked [5]. For this purpose, an additive circuit is needed to detect whether the DLL remains locked or not. In [5], a phase-error compensation (PEC) circuit is used to detect the phase error between the reference clock and the feedback clock in a DLL. Then, the detected phase error is converted to a voltage by an RC low-pass filter. Finally, the output voltage of the RC low-pass filter is compared with a reference voltage. When the output voltage is smaller than the reference voltage, the DLL is still in lock. On the contrary, as the voltage exceeds the reference voltage, the DLL is out-off lock. Then the PFD and CP are turned on for locking the DLL. The PEC needs an analog voltage comparator to compare the output voltage of the RC low-pass filter and the reference voltage. Noise coming from the reference voltage and active devices in the comparator all lead to degradation of jitter performance. Besides, the analog voltage comparator also cost extra power consumption. In this paper, we propose a noise-free all-digital locking detection circuitry (AD-LDC) applied to the DLL for detecting whether the DLL remains locked or not. The AD-LDC contributed no noise to the DLL is also insensitive to process, supply voltage and temperature (PVT) variation.

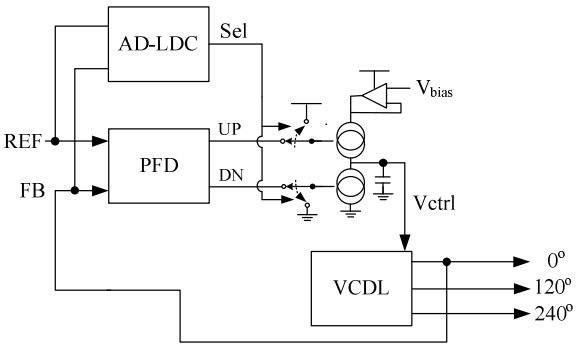


Fig. 1. The proposed open-loop DLL-based multi-phase clock generator.

This paper is organized as follows. Section II describes the architecture of the open-loop DLL-based multi-phase clock generator. Section III describes in detail about the circuits of the open-loop DLL-based multi-phase clock generator. Simulation result is addressed in section V. Finally, a conclusion is remarked.

## II. SYSTEM ARCHITECTURE

Fig. 1 shows the proposed open-loop DLL-based multi-phase clock generator, which is composed of a voltage-control delay line (VCDL), a divider, phase-frequency detector (PFD), charge pump (CP) and an all-digital locking detection circuitry (AD-LDC). The AD-LDC is used to detect whether the DLL remains locked. As the DLL is under locking, output of the AD-LDC (Sel) is set to '0' for opening the DLL. Therefore, noise of PFD and CP will not contribute phase noise at output of the DLL, which greatly reduces the output jitter. On the contrary, as the DLL is out-off lock owing to supply/temperature variations or subtract noise, output of the AD-LDC is set to '1' for relocking the DLL. The AD-LDC opens and closes the DLL by switching the input of the CP. As Sel is '0', the DLL is opened by forcing UP and DN signals of the CP into VDD and ground, respectively. Thus, the CP is turned-off. As Sel is '1', the UP

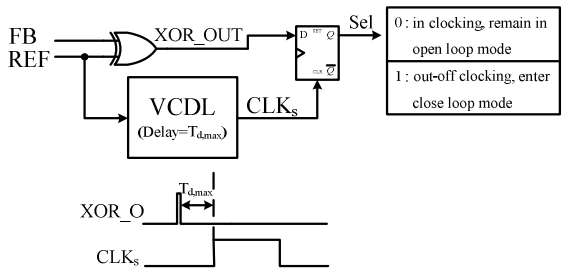


Fig. 2 Block diagram of the AD-LDC.

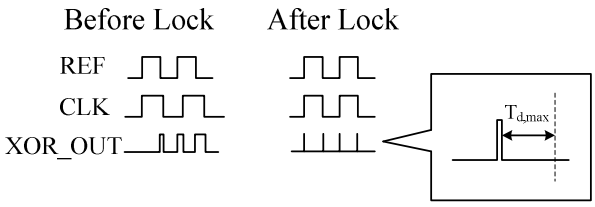


Fig. 3 Time domain waveform of XOR_OUT before and after the DLL is locked.

and DN signals of the CP are reconnected to the output of the PFD. Therefore, the DLL is reclosed for phase locking.

For the most conditions, operating under a stable supply voltage provided by a supply regulator and a stable operating temperature, the DLL will be under locked even the loop is opened. As operating under a worse environment, the AD-LDC can be very sensitive to the phase error happened in the DLL. Therefore, the DLL can be relocked within one reference period, which results in good system reliability.

## III. CIRCUIT DESIGN

### *A. All-digital locking detection circuitry (AD-LDC)*

Fig. 2 shows block diagram of the all-digital locking detection circuitry (AD-LDC). Composed by a XOR, a voltage control delay line (VCDL) and a D-flip-flop, the AD-LDC is designed to detect whether the DLL is locked in time domain. The XOR compares the phase between the feedback clock (FB) and reference clock (REF), and generates an output of a pulse-width modulated signal. The VCDL produces a clock signal ($CLK_s$) which delays the REF with a time of $T_{d,max}$. Then the CLK is used to sample the output signal of the XOR (XOR_OUT) in time domain. As the pulse width of XOR_OUT is less than $T_{d,max}$, the output of the AD-LDC is '0'. Then we decide the DLL is locked. On the contrary, as the pulse width of XOR_OUT is larger than $T_{d,max}$, the output of the AD-LDC is '1'. Then we decide the DLL is unlocked. Therefore, the time delay of the VCDL ($T_{d,max}$) plays a role of threshold time to decide whether the DLL is locked and can be tuned by a control voltage. Fig. 3 shows the time domain waveform of XOR_OUT before and after the DLL is locked. The VCDL composed by a chain of an inverter with a varactor load is shown in Fig. 4.

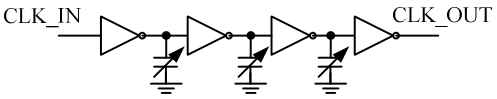


Fig. 4 The VCDL in the AD-LDC.

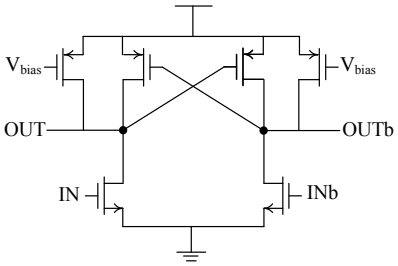


Fig. 5 Schematic of the delay cell.

### *B. DLL-based multi-phase clock generator*

The DLL-based multi-phase clock generator is composed by a VCDL, a PFD and a supply-regulated CP. The VCDL is consisted by three delay cells. Therefore, clocks with phase rotations of $0^o$, $120^o$ and $240^o$ can be generated. Fig. 5 shows the schematic of the delay cell. Cross-coupled pair is used in the delay cell for power saving and improving phase noise performance [6]. The PFD is designed in tri-state architecture. Owing to the DLL is opened-loop as operating in the nominal state; a supply-regulated CP is needed to keep an unvaried $V_{ctrl}$ for the VCDL as supply voltage is varied. Fig. 6 shows the schematic of the supply-regulated CP. The supply-regulated CP also features elimination of current mismatch. A replica of the output branch is added. Therefore, the current sources (M1-M2) are always turn-on and un-affected by the switching pulses. Additionally, OP1 is used to keep $V_R$ following the CP output voltage. Thus both current sources are balance whether in the charging or discharging phase. Thanks to OP2, the $V_b$ in the bias branch will track the CP output voltage, thus the $r_{ds}$ variation of current sources (M1-M4) are cancelled over the entire CP output range. Moreover, all switches (SW1-SW6) in this CP are implemented in transmission-gate configuration. In the conventional CP design, the switches are designed in n-channel or p-channel configuration, therefore the UP and DN pulses see the unbalance loads. Owing to the transmission gate configuration, the unbalance problem is solved. Besides, the transmission gate configuration leads to no DC drop for enlarging the CP output voltage range.

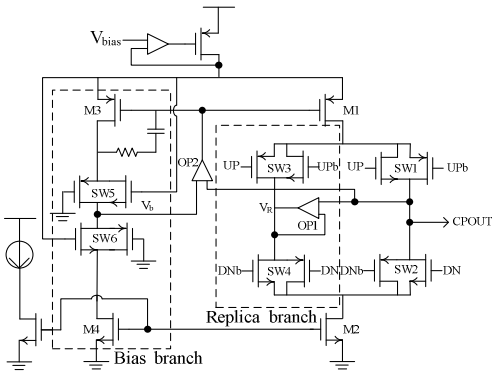


Fig. 6 The schematic of the current-mismatch free, supply-regulated charge pump.

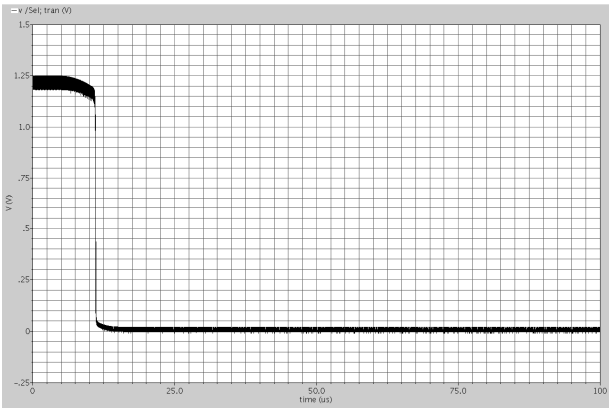

Fig. 8 Time domain waveform of the output of the AD-LDC.

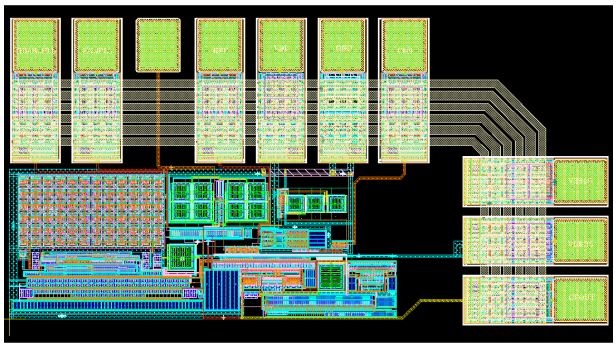

Fig. 7 Layout of the open-loop DLL-based multi-phase clock generator.

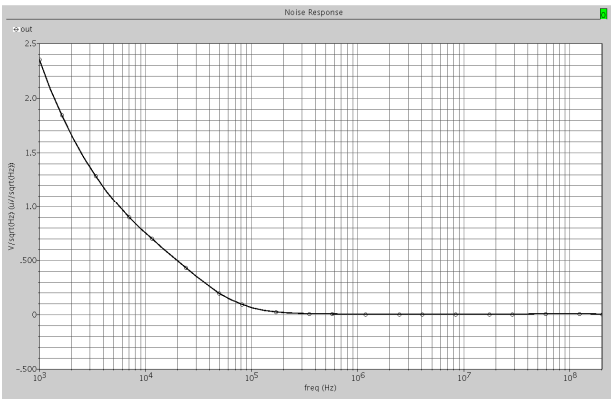

Fig. 9 The output noise voltage of the detector (PFD+CP) as the DLL operates under open-loop mode.

## IV. Simulation Result

Fig. 7 shows the layout of the open-loop DLL-based multi-phase clock generator. The whole chip has active area of 0.01 $mm^2$. Fig. 8 shows time domain waveform of the output of the AD-LDC, Sel. As Sel is 1.2 V (logic '1'), the DLL is closed-loop to lock the output clock by the reference clock. On the contrary, as Sel is 0 V (logic '0'), the DLL is opened-loop. In the Fig. 8, before 11 $\mu$ s, there is a large phase error detected by the AD-LDC resulting a time-domain pulse wider than $T_{d,max}$ ( control by the VCDL in the AD-LDC). After 11 $\mu$ s, the phase error detected by the AD-LDC is less than the $T_{d,max}$. Thus the DLL is opened-loop to eliminate noise contributed by the PFD and the CP which result in a better jitter performance. Fig. 9 shows the output noise voltage of the detector (PFD+CP) as the DLL operates under open-loop mode. The output noise voltage contributed by the thermal noise sources (frequency above 600 KHz in Fig. 9) in the detector can be eliminated by switching off UP and DN transistors in the CP. Fig. 10 shows phase noise performance of the 400 MHz clock source. The DLL performs a low-pass response to the detector noise and a high-pass frequency response to the VCDL. Owing to the most noise contributed by the detector is eliminated by open-loop the DLL. For minimizing output jitter of the DLL, a capacitor is placed in the output of CP to form a one-pole filter with corner frequency of 100 MHz for eliminating the most noise of the 400 MHz clock source. The simulated phase noise of the DLL in open-loop mode is shown in Fig. 11. Therefore, a 500 fs rms jitter can be found by integrating the phase noise. Performance summary and comparison other works are listed in Table I.

## V. Conclusion

A DLL-based multi-phase clock generator operating in open-loop mode is designed in 0.13 $\mu$m CMOS process. Unlike previous design detects whether the DLL is locked by analog circuits in voltage domain, a proposed noise-free all-digital locking detection circuitry (AD-LDC) is used to detect whether the DLL is locked in the time domain which leads to no analog design effort and avoids noise contributed by the detection circuitry. An rms jitter of 500 fs can be achieved in

Table I Performance summary and comparison

| | JSSC'02 [1] | JSSC'02 [2] | ISSCC'05 [3] | VLSI Symp.'07 [4] | JSSC'09 [6] | This Work |
|---|---|---|---|---|---|---|
| Type | Analog | Analog | Analog | Digital | PEC (Analog) | AD-LDC (Digital) |
| Process | 0.18 µm | 0.35 µm | 0.35 µm | 0.13 µm | 90 nm | 0.13 µm |
| Frequency | 2 GHz | 1.1 GHz | 1.8 GHz | 1.6 GHz | 2 GHz | 0.4 GHz |
| Supply | 1.8 V | 3.3 V | 3.3 V | 1.2 V | 1 V | 1.2 V |
| Jitter (RMS) | 1.6 ps (@2GHz) | 2 ps (@1.1GHz) | 1.8 ps (@1.8GHz) | 1.4 ps (@1.6GHz) | 1.6 ps (@2 GHz) | 0.5 ps (@0.4 GHz) |
| Area | 0.05 mm2 | 0.07 mm2 | 0.07 mm2 | 0.037 mm2 | 0.037mm2 | 0.01 mm2 |
| Power | 12 mW | 42.9 mW | 86.6 mW | 6 mW | 7 mW | 14 mW |

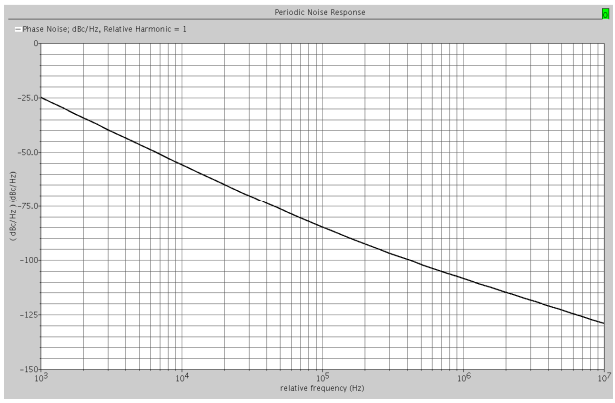


Fig. 10 Phase noise performance of the 400 MHz clock source.

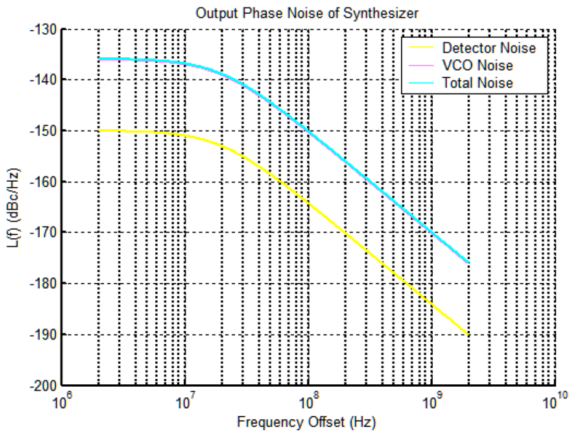


Fig. 11 The simulated phase noise of the DLL in open-loop mode

this design. The DLL-based multi-phase clock generator can be used as a clock source for high speed ADCs/DACs and wireline transceivers.

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