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Low-Power Fast-Settling Low-Dropout Regulator Using a Digitally Assisted Voltage Accelerator for DVFS Application

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Abstract. This paper presents a low-power fast-settling low-dropout regulator (LDO) using a digitally assisted voltage accelerator. Using the selectable-voltage control technique and digitally assisted voltage accelerator significantly improves the transition response time within output voltage switched. The proposed LDO regulator uses the selectable-voltage control technique to provide two selectable-voltage outputs of 2.5 V and 1.8 V. Using the digitally assisted voltage accelerator when the output voltage is switched reduces the settling time. The simulation results show that the settling time of the proposed LDO regulator is significantly reduced from 4.2 ms to 15.5 μs. Moreover, the selectable-voltage control unit and the digitally assisted voltage accelerator of the proposed LDO regulator consume only 0.54 mW under a load current of 100 mA. Therefore, the proposed LDO regulator is suitable for low-power dynamic voltage and frequency-scaling applications.

INTRODUCTION

More system designs on a chip correspond to increased energy consumption. The low voltage, low quiescent current, and low dropout-voltage of the low-dropout (LDO) regulator are important. The dynamic voltage and frequency-scaling (DVFS) technique [1]-[3] saves power consumption in SoC systems and provides high and low output voltages. For DVFS applications in mobile systems [4]-[6], the LDO is one of the optimal supply voltage principle of operation is compared the difference of V_{ref} and V_{fb}. The LDO uses analog signals to control power MOS to operate in the saturation or linear regions. High-accuracy output voltage, low noise, simple architecture, and fast

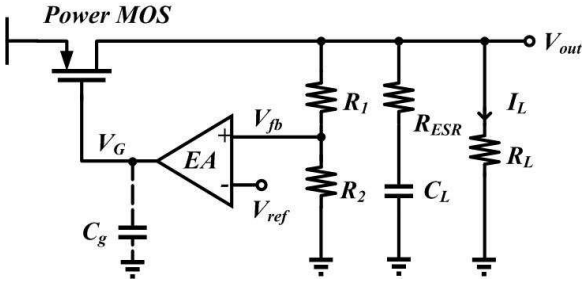


Fig. 1 Conventional LDO circuit structure.

transient response properties are characteristics of the LDO regulator. Dividing the compensation methods into on-chip [7]-[9] and off-chip [10]-[11] improve LDO stability and response times. The off-chip compensation method [10]-[11] improves the error amplifier (EA) or buffer-stage driving capability with the compensation component RESR.

This study presents a novel fast-settling LDO regulator with a selectable-voltage control unit and digitally assisted voltage accelerator.

Operation Principle for the Proposed LDO

Fig. 2 shows the proposed LDO with two selectable-voltage outputs. Output signals X_1 and X_0 of the decoder (*Dec*) switch on NMOS transistors M_1 and M_2 and generate two types of output voltage, V_L and V_H. To improve the transient time of the output voltage, this study proposes the digitally assisted voltage accelerator to increase the charge/discharge current and compares the voltage difference between the reference voltage (V_{ref}) and the feedback voltage (V_{fb}).

Selectable-Voltage Control Unit

As shown in Fig. 2, the selectable-voltage control unit is composed of two NMOS transistors (M_1 and M_2), three feedback resistors (R_1, R_2, and R_3), and one decoder (*Dec*). Fig. 3 shows the operation principle of the selectable–voltage control unit. When signal *Sel* is high, output signals X_1 and X_0 of the decoder (*Dec*) are low and high, respectively. When NMOS M_2 is switched on, the voltage of V_{fb} increases slightly, and vice versa.

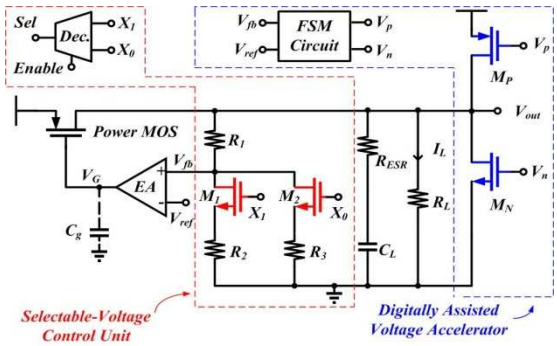


Fig. 2 Circuit structure of the proposed LDO regulator

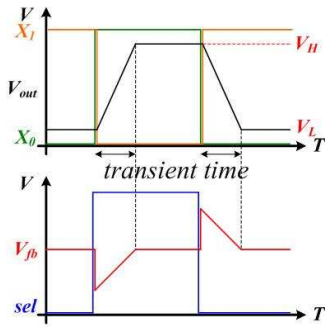


Fig. 3 Operation principle of the selectable-voltage control unit

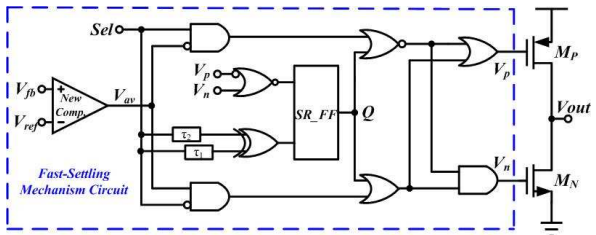


Fig. 4 Circuit structure of the digitally assisted voltage accelerator

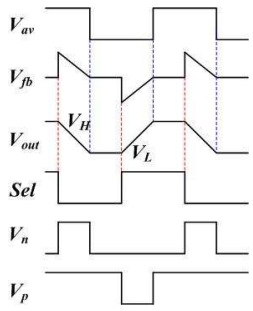


Fig. 5 Operation principle of the digitally assisted voltage accelerator

Digitally Assisted Voltage Accelerator

Fig. 4 shows that the digitally assisted voltage accelerator is composed of a fast-settling mechanism circuit and extra push/pull MOS transistors (M_P and M_N). The following paragraphs discuss the operation principle and details of the circuit structures.

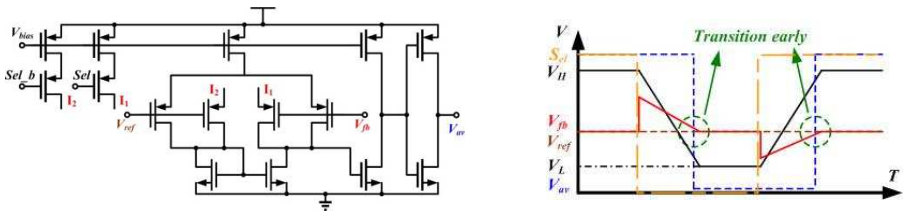
Fig. 5 shows the operation principle of the digitally assisted voltage accelerator. When signal *Sel* moves from high to low, voltage V_{fb} increases slightly. Output voltage V_n then increases from low to high to switch on extra pull MOS transistor M_N, which reduces V_{out} falling time.

Fast-Settling Mechanism Circuit

As shown in Fig. 4, the fast-settling mechanism circuit is composed of the new comparator, an SR latch, and digital logic gates. τ_2 of the delay time is twice τ_1. Fig. 6(a) shows the circuit structure of the new comparator circuit. Two additional discharge currents I_1 and I_2 generate the different transient points. Fig. 6(b) is the operation principle of the new comparator. Voltage V_{out} decreases from V_H to V_L when the *Sel*/*Sel_b* signals are low/high. If V_{fb} is lower than $V_{ref}+\Delta V$, voltage V_{av} decreases from high to low. Therefore, using output voltage V_{av} of the new comparator switches off the digitally assisted voltage accelerator.

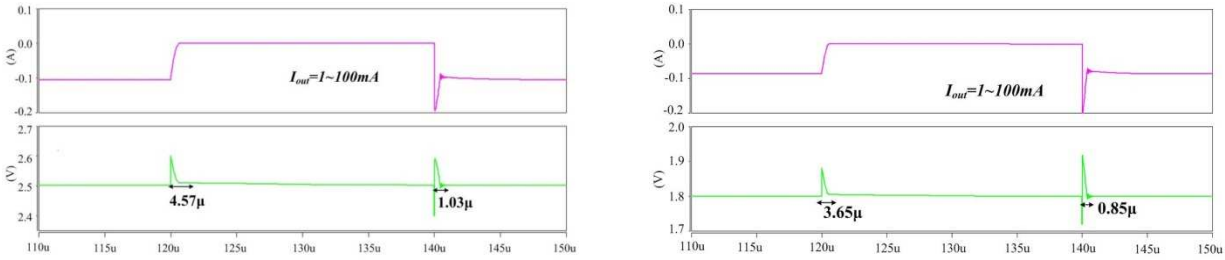
Simulation and Experiment Results

The proposed LDO with a digitally assisted voltage accelerator and selectable-voltage control was designed and simulated using a TSMC 0.35 μm CMOS process. The two selectable-voltage output levels of the proposed LDO output are regulated at 2.5 V (V_H) and 1.8 V (V_L). Fig. 7 shows the simulation results of the load regulation transient response of the proposed LDO regulator. As



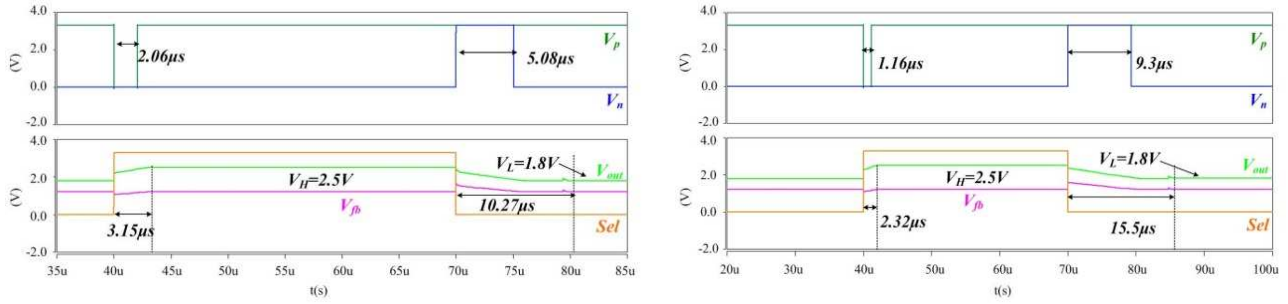
(a) (b)

Fig. 6 (a) The circuit structure of the new comparator circuit (b) The operation principle of the new comparator



(a) (b)

Fig. 7 The simulation of load regulation when load current changes. (a) I_{out} changes from 1 mA to 100 mA at V_{out}=2.5 V. (b) I_{out} changes from 1 mA to 100 mA at V_{out} =1.8 V.



(a) (b)

Fig. 8 The output voltage of LDO changes from 1.8 V to 2.5 V, and vice versa. (a) A heavy load (100 mA). (b) A light load (1 mA)

Table 1 Performance comparisons with previous research

Parameter	Comparison		
	2008 [19]	2005 [25]	**This Work**
Technology [μm]	0.35	0.09	**0.35**
Supply Voltage [V]	2	1.2	**3.3**
Output Voltage [V]	1.8	0.9	**1.8 / 2.5**
C_{out} [μF] / ESR [ohm]	1 / N.A.	0 / N.A.	**2.5 / 1**
I_Q [mA]	0.027	6	**0.0217**
Settling Time [μs] (Load Regulation)	5	N.A.	**4.57**
Settling Time [μs] (voltage changed)	N.A.	N.A.	**15.5**
Max. Load [mA]	150	100	**100**
Load Regulation [μV/mA]	467	900	**35.9**
T_R# [μs]	0.467	0.00054	**0.08975**
FOM# [ns]	0.084	0.032	**0.019**

#Adopted from [25], $T_R=C_{OUT}\times\Delta_{VOUT}/I_{OUT}(MAX)$ and $FOM=T_R\times I_Q/I_{OUT}(MAX)$

shown in Fig. 7(a), when load current Iload is changed from 1 mA to 100 mA at Vout = 2.5 V, the output voltage stabilizes within 4.57 μs. When load current Iload is changed from 1 mA to 100 mA at Vout = 1.8 V, as shown in Fig. 7(b), the output voltage stabilizes within 3.65 μs. Therefore, the load regulation of the proposed LDO regulator is 35.9 μV/mA.

Fig. 8 shows that the output voltage switches from 1.8 V to 2.5 V in heavy load (100 mA) and light load (1 mA) conditions, respectively. As shown in Fig. 8(a), when signal *Sel* increases from low to high, the V_p signal decreases from high to low and switches on the extra push PMOS transistor M_P to increase the V_{out} charge speed. Therefore, when output voltage V_{out} increases from 1.8 V to 2.5 V, the rising time under a load current of 100 mA is 3.15 μs. Therefore, output voltage V_{out} decreases from 2.5 V to 1.8 V with a falling time of 10.27 μs at a 100 mA load current.

Fig. 8(b) shows that when signal *Sel* changes state, the V_p/V_n signal increases/decreases from high/low to low/high which switches on extra push/pull MOS transistors M_P and M_N to improve the V_{out} transition response time. When output voltage V_{out} decreases from 2.5 V to 1.8 V, the maximal settling time of V_{out} is 15.5 μs.

Table 1 shows a comparison of the simulation results to previous research. The simulation results show that the settling time of the conventional LDO regulator without using a fast-settling mechanism is 4.2 ms. The settling time with a fast-settling mechanism is only 15.5 μs.

Conclusion

This paper proposes a novel fast-settling LDO regulator with two selectable-voltage outputs for DVFS applications.

The digitally assisted voltage accelerator and the selectable-voltage control unit techniques are used to achieve two selectable selectable-voltage outputs (2.5 V and 1.8 V) and a fast transient response time. According to the simulation results, the quiescent current is only 21.7 μA. Moreover, the selectable-voltage control unit and the digitally assisted voltage accelerator of the proposed LDO consume only 0.54 mW under a load current of 100 mA. Therefore, the proposed LDO regulator is suitable for low-power and DVFS applications.

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