A 0.3V 1kb Sub-Threshold SRAM for Ultra-Low-Power Application in 90nm CMOS

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***Abstract*—Ultra-low power device is very popular in recent years because of some applications like medical device and communications. For the ultralow-power consideration, the crucial in SRAMs are stability and reliability. In conventional 6T SRAMs is hard to achieve reliability in sub-threshold operation. Hence, some researchers have considered different configuration SRAMs cell for sub-threshold operations having single-ended 8T, 9T, 10T or differential pair structure for improved stability and reliability. In this paper, the purposed 10T differential bit-cell that effectively separates read and write operation path, therefore achieving high stability. The purposed 1kb 10T sub-threshold SRAM (64x16) implemented in 90nm CMOS technology operates at 10MHz at 300mV with measured power consumption of 1.48µW and energy consumption of 0.296pJ for one write and one read operation.**

I. INTRODUCTION

For power-constrained applications, such as wireless sensor networks, implantable devices, and medical apparatus, sub-threshold SRAMs and logics are popular be used to reduce power consumption. However, with the advances in process technologies, designing reliable sub-threshold circuit have to face some challenges, such as process variation and threshold voltage variation due to doping fluctuation. These factors all restrict circuit operation especially in sub-threshold region.

In the sub-threshold region, conventional 6T SRAM cells have weak read stability or writablity [1]. Read stability and waritablity are the part of focus on SRAM design requirements; it is very difficult to operate the 6T SRAM in the sub-threshold region. For increase cell stability, single-ended 8T [5], 9T [6] or 10T [1] and differential read scheme 10T [2] SRAMs have been explored. In these scheme of memory cell, all of these structure ensures read SNM to be almost the same as hold SNM, that improving read stability apparent. As supply power scales down, soft-error rate (SER) [7] increases by 18% for every 10% VDD reduction. In the sub-threshold region, SER can be much larger than that in the super-threshold region. However, in sub-threshold SRAMs cell design, some critical point that we have to face: read and write stability, bit-line leakage reduction, SNM.

In this paper, purposed 10T SRAM utilization read and write separation path to upgrade performance. We use the bit-interleaved scheme to solve the problem of SER. An overview of this paper, section Ⅱ presentation proposed 10T differential SRAM and the mode of operation. In the section Ⅲ, bit-interleaving scheme discussed. Then at the section Ⅳ describe the architecture of the SRAM. The final section is conclusions of this work.

II. PROPOSED 10T SUB-THRESHOLD SRAM CELL

The proposed 10T differential SRAM cell is shown in Fig. 1. In the read operation, word-line (WL) is enabled and virtual ground (VGND) decreases to 0V during the process of the read mode, and write word-line (WWL) remains disable. The disable WWL makes storage node Q and QB decoupled from BL and BLB when read access. Because of this isolation, the read SNM can be almost same with conventional 6T SRAM cell. The SNM of proposed 10T SRAM is shown in Fig. 2.

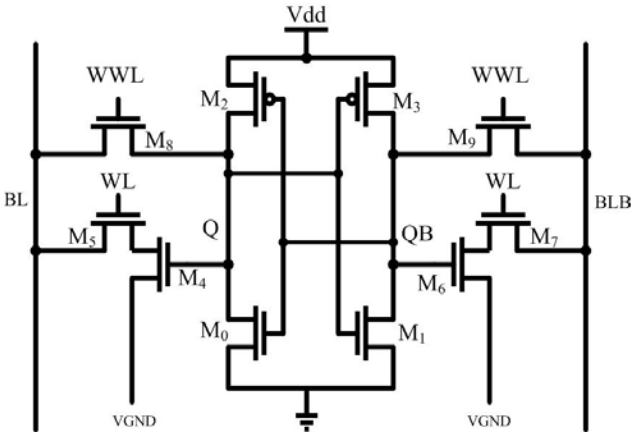

Fig. 1. Proposed 10T SRAM cell

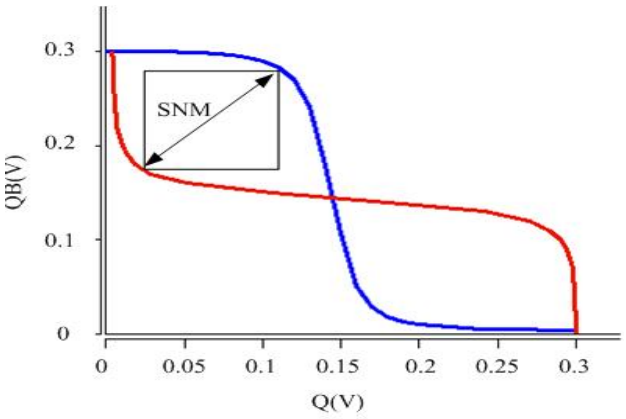

Fig. 2 . SNM of proposed 10T cell

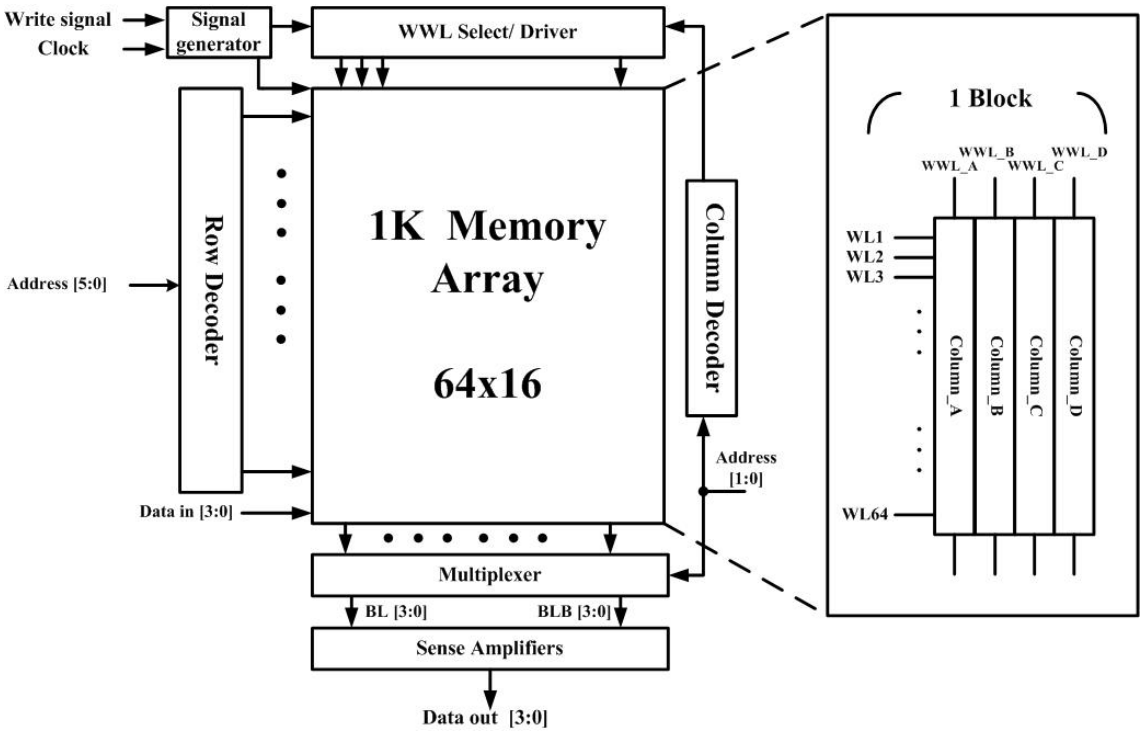

Fig. 3 . Architecture of proposed SRAM

Depending on the storage data in node Q and QB, corresponds to the BL of nodes to access the data 1 will discharging after WL is enable. Due to this differential read structure, the read value will be the inverted signal of the storage data.

In the write operation, WWL is enable to transfer data into the storage node from bit-lines, WL is enable and VGND keep in high can reduce bit-line leakage during write mode. It is hard to write data “1” than write data ”0” because our transfer transistor M4 and M5 in Fig. 1 are NMOS, so the access time we calculated is almost the same as the time to write data “1” . For a successful write, the bit-cell becomes monostable compel the internal storage node voltages to the correct values. In this work, we write data “1” by pull down BL then internal node Q discharge. Thus, when read the bit, BL keep in high by M9 and BLB pull down from M7 then we read data “1” to output.

When we wrote data “1” by pulling down BL, the internal node Q discharged to 0. Thus, when reading the bit, a high BL was maintained by M4 and BLB was pulled down from M6; subsequently, we read data “1” to output. The procedure was the same to write data “0”; that is, we pulled down BLB, and the internal node QB subsequently discharged to 0. Therefore, when reading the bit we wrote, a high BLB was maintained by M6, and BL pulled down from M4; subsequently, we read data “0” to output. This study required 21.66 ns to complete the write operation and 41.91 ns to complete the read operation at 300 mV and a typical corner. Thus, the proposed SRAM can operate at 10 MHz clock frequency at 300 mV and typical process (TT) corner.

III. BIT-INTERLEAVED FOR SOFT-ERROR

According to [7], we can see that soft-error rate (SER) increases by 18% for every 10% VDD reduction, so the SER in 0.3V supply voltage will much higher than in 1V supply voltage. Soft error occurred by the reduction of critical charge in weak inversion region is an issue. A soft-error may flip adjacent multiple bits simultaneously. Therefore, error correction coding (ECC) and bit-interleaving are the solutions to soft-error for sub-threshold SRAM. ECC techniques can detect and correct single bit errors; bit-interleaving can let us handle multiple bit soft-errors efficiently.

Soft-error is a signal or data which is wrong, but is not assumed to imply such a mistake. The soft-error bit only correction when the bit is written next time or soft-errors may affect data but not change to the circuit. Since continuous bit-cells could be corrupted at one injection, the interleaving scheme is good solution for the effect of soft error will associated with different logical words. In fact, most soft-error happened is single-bit error. For single-bit error correction would be quite effective by implementing ECC. According to [4], ECC can reduce failure rate by over four orders of magnitude. But in SRAM may encounter more bit-error in one word because of continuous bit-cells structure. So the better method to reduce SER in SRAM is bit-interleaved scheme.

In this architecture, WL is shared by the cells in a row, and WWL is shared by the cells in a column. In proposed SRAM, WWL signal is synthesis by column decoder and WL pulse, only if column be selected and WL enable that the selected cell

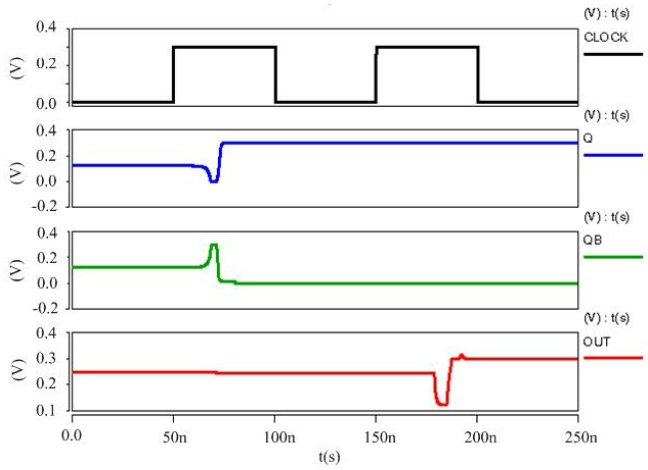

Fig. 4. Simulation Result in a write/read Operation Cycle (write "1" & read "1")

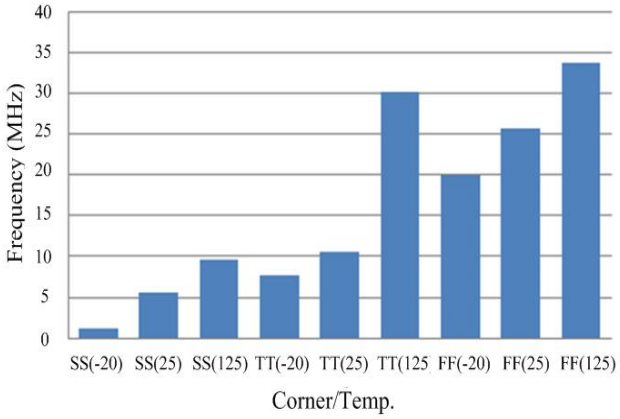

Fig. 6. Max operating frequency versus corner with different temperature

can be written. Thus there are no disturbances for the half-selected bit-cells.

IV. ARCHITECTURE OF THE 10T SRAM

The architecture of proposed sub-threshold 10T SRAM is shown in Fig. 3. It is composition by address decoders, write circuit, WL and WWL driver, signal generator, sense amplifier, memory cell array, and multiplexer. The memory cell array composed in bit-interleaved scheme that described in the previous section.

Address decoder in a SRAM is devices which provide n-bit address by 2^n address line in SRAM cell array. In this work, we configure 6-bit address for row decoder to generate 64 word lines, and 2-bit to 4 select signal for WWL_A, WWL_B, WWL_C, WWL_D. Due to row decoder have 6-bit that row decoder must use 6 input AND gate, but it has a problem that the number of fan-in too much in a single logic gate, makes gate delay increases. So in this case, we proposed two stage decoder (4x3) to decrease gate delay.

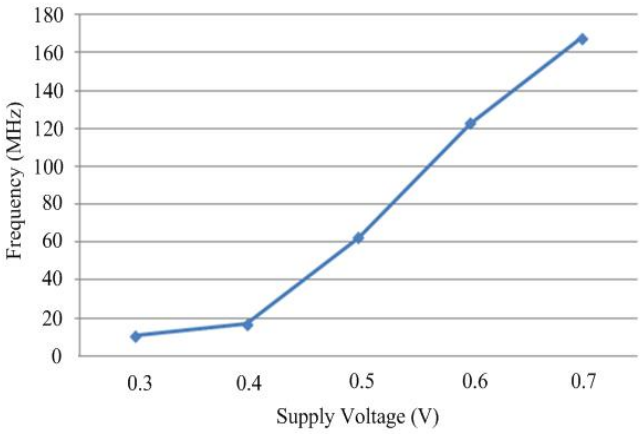

Fig. 5. Maximum operating frequency versus supply voltage

For proposed SRAM, signal generator produce WP (write pulse), RP (read pulse), and EN. Write pulse is used to control write circuit and be a precharge controller needed in each BL. Read pulse is used to control virtual ground. EN is an enable signal to control transmission gate of each BL and sense amplifiers, it is only generate after read pulse.

V. CONCLUSIONS

In this paper, a 1kb 10T sub-threshold SRAM implemented in a 90nm CMOS technology with differential read scheme and bit-interleaving scheme is proposed. By the simulation results, it is achieves operation frequency of 10MHz at 300mV is shown in fig. 4; and the analysis between operation frequency and supply voltage is shown in Fig. 5. And Fig. 6 shown the operating frequency versus corner with different temperature. The average operation power consumption is 1.48μW and energy consumption is 0.296pJ at 10MHz and 300mv; standby power consumption is 0.749μW. Table I compares the results with some recently reported SRAMs.

TABLE I .
COMPARISON OF RESULT

	[3]	[5]	This Work
Technology	90nm CMOS	90nm CMOS	**90nm CMOS**
Density	4kb	4kb	**1kb**
Cell number per BL	256	256	**64**
Cell Type	8T	8T	**10T**
VDD min	0.2V	0.38V	**0.3V@27℃**
Performance	6MHz @0.2V	6MHz @0.38V	**10MHz @0.3V;27℃**
Power consumption	10.4 μW	2.99 μW	**1.48μW**
One write/read Operation Energy	3.47pJ	0.998pJ	**0.296pJ**

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