A 300 mV 10 MHz 4 kb 10T Subthreshold SRAM for Ultralow-Power Application

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Abstract—**Ultralow-power devices have become popular in recent years because of their use in a number of applications, such as medical devices and communications. For ultralow-power consideration, the crucial factors in SRAMs are stability and reliability. A number of researchers considered various configurations of bit-cells for SRAMs for subthreshold operations, with differential pair structure and single-ended 8T, 9T, and 10T to improve stability and reliability. This paper proposes a 10T differential bit-cell that can effectively separate the read and write operation paths. We used a high Vth NMOS in the write operation path to reduce the bit-line leakage current. We also used virtual ground (V_Vss) to reduce the bit-line leakage to ensure that the data can be read correctly. The proposed SRAM was composed of 16 blocks, and each block had four columns and 64 cells per bit-line in a column. This study implemented a 4 kb 10T subthreshold SRAM in 90 nm CMOS technology operating at 10 MHz and 300 mV, which exhibited power consumption of 4.25 µW and energy consumption of 0.85 pJ for one write and one read operation.**

Keywords: SRAM; Subthreshold; Ultralow-Power

I. INTRODUCTION

Subthreshold SRAMs and logics are commonly used for power-constrained applications, such as wireless sensor networks, implantable devices, and medical apparatuses, to reduce power consumption. However, with the advances in process technologies, the design of reliable subthreshold circuits experience a number of challenges, such as process variation and threshold voltage variation caused by doping fluctuation. These factors restrict circuit operation, especially in the subthreshold region.

In the subthreshold region, conventional 6T SRAM cells exhibit weak read stability or writability [1]. Read stability and writability are the focus of SRAM design requirements. It is difficult to operate a 6T SRAM in the subthreshold region. Single-ended 8T [7], 9T [8], or 10T [2], and differential read scheme 10T [9] SRAMs have been explored to increase cell stability. TABLE I shows a comparison of various SRAM bit-cells. All of these memory cell schemes ensure that the read SNM is almost the same as the hold SNM, which improves read stability. As the supply power scales down, the soft-error rate (SER) [10] increases by 18% for every 10% VDD reduction. In the subthreshold region, the SER can be larger than that in the super-threshold region. However, read and write stability, bit-line leakage reduction, and SNM are crucial points that must be considered in the cell design of subthreshold SRAMs.

This study separated the 10T SRAM read and write path to upgrade performance and reduce bit-line leakage with high Vth NMOS and virtual ground. We used the bit-interleaved scheme to solve the problem of SER. The remainder of this paper is organized as follows: Section II presents the proposed 10T differential SRAM and the mode of operation; Section III introduces the bit-interleaving scheme; Section IV shows the architecture of the SRAM; and lastly, Section V offers a conclusion.

II. PROPOSED 10T SRAM CELL

A 10T differential SRAM cell is shown in Fig. 1. The proposed 10T cell comprises a latch and two pass-transistors, M8 and M9, which is the path of write. It is similar to the traditional 6T memory cell; however, we used a high Vth NMOS in M8 and M9 to effectively reduce the bit-line leakage in the read and hold mode. Moreover, M4 and M6 are controlled by the storage data. When storage node Q accesses data "1" in the read mode, the bit-line discharges from M4 to the ground. Thus, the input data differs from the internal storage data; therefore, the output data are the same as the input data.

Furthermore, M5 and M7 are controlled by the word-line. In hold mode, M4 and M5 (M6 and M7) can be a stacked structure to reduce the bit-line leakage power. The proposed 10T SRAM cell had two word-lines, which are write word-line (W_WL) and word-line (WL), differential bit-line (BL) and bit-line bar (BLB), and virtual ground (V_Vss).

TABLE I. COMPARISON OF VARIOUS SRAM BITCELLS

SRAM Type	**5T [11]**	**6T [13]**	**7T [12]**	**8T [2]**	**9T [3]**	**10T [proposed]**
Read	Single Ended	Diff.	Diff.	Single Ended	Single Ended	Diff.
#WL	1	1	1	2	2	2
#BL	1	2	2	1	1	2
#PMOS	2	2	2	2	3	2
#NMOS	3	4	5	6	6	8

※Diff.: Differential

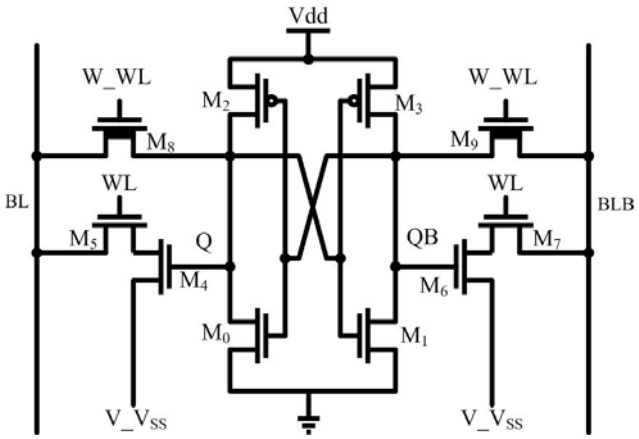

Figure 1. Proposed 10T SRAM cell.

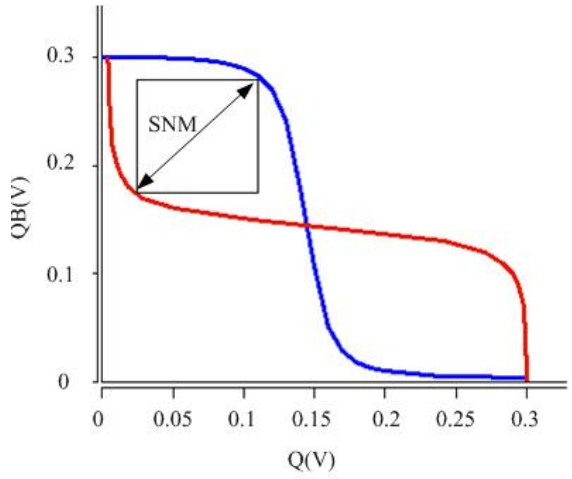

Figure 2. SNM of the proposed SRAM cell.

A. *Read Operation*

In the read operation, the word-line (WL) is enabled, the virtual ground (V_Vss) decreases to 0 V during the process of the read mode, and the write word-line (W_WL) remains disabled. The disabled W_WL causes the storage nodes Q and QB to decouple from the bit-line (BL) and bit-line bar (BLB) during read access. Because of this isolation, the read SNM is almost the same as that in a conventional 6T SRAM cell. The SNM of the proposed 10T SRAM is shown in Fig. 2. The virtual ground ensures that the data can be read successfully in subthreshold operations. Depending on the storage data in nodes Q and QB, the BL of nodes to access the data "1" will discharge after WL is enabled. Because of this differential read structure, the read value will be the inverted signal of the storage data.

B. *Write Operation*

In the write operation, W_WL is enabled to transfer data into the storage node from the bit-lines, WL is disabled, and a high V_Vss is maintained to reduce bit-line leakage during write mode. It was more difficult to write data "1" than data "0" because our transfer transistors, M8 and M9 (Fig. 1), were NMOS; therefore, we calculated the access time

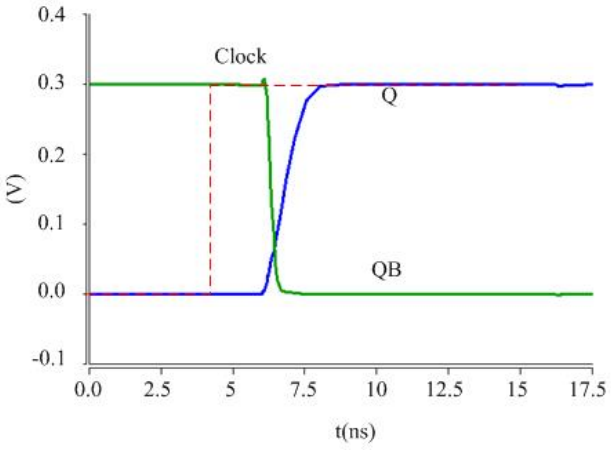

Figure 3. The simulation result of a single cell write operation.

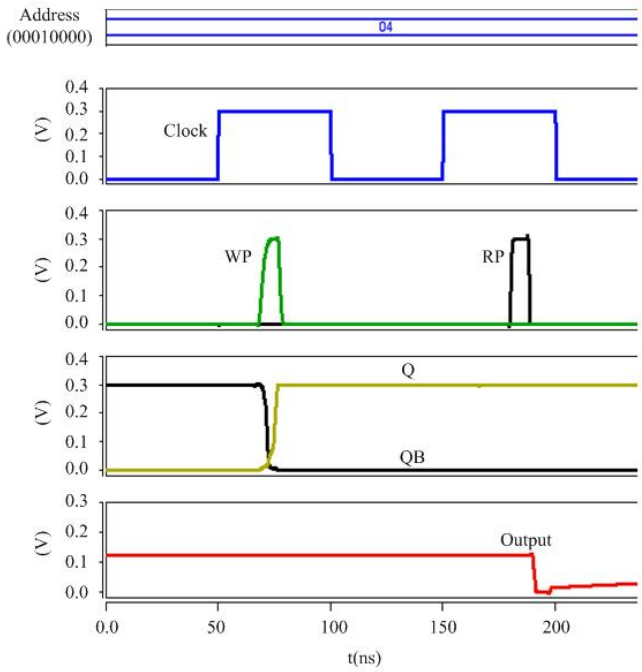

Figure 4. The simulation result of an operation cycle (one column).

according to the time to write data "1." The variation of storage nodes Q and QB after write "1"operation is shown in Fig 3. According to the single-cell simulation, the internal node's rising time was 1.2691 ns and its falling time was 330.84 ps; therefore, we designed the write word-line pulse to exceed 2 ns to reduce power consumption. For a successful write, the bit-cell becomes monostable, which compels the internal storage node voltages to the correct values.

When we wrote data "1" by pulling down BL, the internal node Q discharged to 0. Thus, when reading the bit, a high BL was maintained by M4 and BLB was pulled down from M6; subsequently, we read data "1" to output. The procedure was the same to write data "0"; that is, we pulled down BLB, and the internal node QB subsequently discharged to 0. Therefore, when reading the bit we wrote, a high BLB was maintained by M6, and BL pulled down from

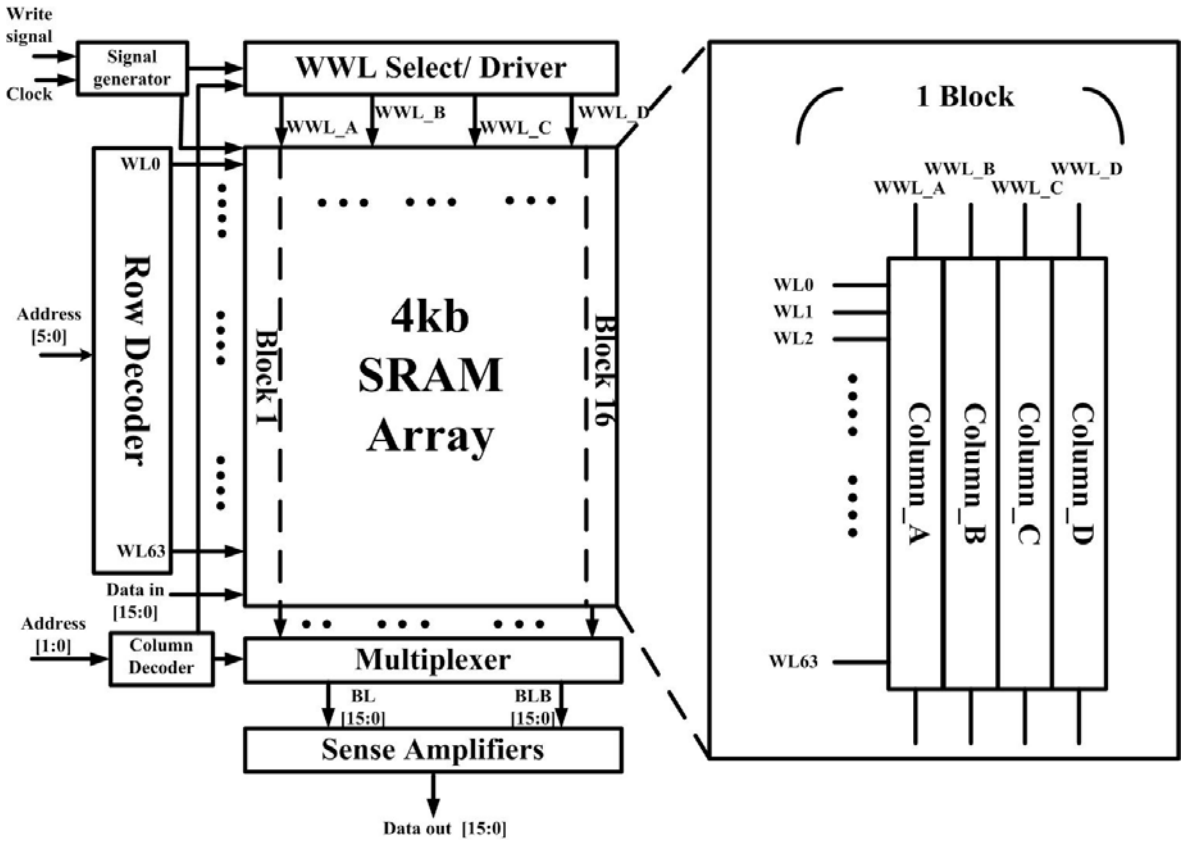

Figure 5. Architecture of the proposed SRAM and block structure of the proposed SRAM.

M4; subsequently, we read data “0” to output. Fig 4. shows the simulation result in an operation cycle (write “0” and read “0”). This study required 21.66 ns to complete the write operation and 41.91 ns to complete the read operation at 300 mV and a typical corner. Thus, the proposed SRAM can operate at 10 MHz clock frequency at 300 mV and typical process (TT) corner.

III. BIT-INTERLEAVED FOR SOFT-ERROR

According to [10], the soft-error rate (SER) increases by 18% for every 10% supply voltage reduction; therefore, the SER at a 0.3 V supply voltage will be higher than that at a 1.2 V supply voltage. A soft-error occurred because of the reduction of critical charge in the weak inversion region. A soft-error may flip adjacent multiple bits simultaneously. Therefore, error correction coding (ECC) and bit-interleaving are used as solutions to the soft-error for subthreshold SRAMs. The ECC techniques can detect and correct single bit errors; bit-interleaving enables efficient management of multiple bit soft-errors.

A soft-error is a signal or data that are incorrect, but not assumed to imply a mistake. The soft-error bit is only corrected when the bit is written the next time, and soft-errors may affect data, but cannot change the circuit. Because continuous bit-cells can be corrupted at one injection, the interleaving scheme is an optimal solution when soft errors associate with different logical words. Most soft-errors are single-bit errors. The implementation of ECC is effective for single-bit error correction. According to [6], ECC can reduce the failure rate by over four orders of magnitude. However, an SRAM may encounter more bit-errors in one word because of the structure of continuous bit-cells. Therefore, the bit-interleaved scheme is a superior method to reduce SER in an SRAM. In this architecture, WL is shared by the cells in a row, and WWL is shared by the cells in a column. In the proposed SRAM, the WWL signal is synthesized by the column decoder and WL pulse if the column be selected and WL can be enabled to write on the selected cell. Thus, disturbances occur for the half-selected bit-cells.

IV. ARCHITECTURE OF THE 4K SRAM

The architecture of the proposed subthreshold 10T SRAM is shown in Fig. 5. It comprises address decoders, a write circuit, WL and WWL drivers, a signal generator, a sense amplifier, a memory cell array, and a multiplexer. The memory cell array comprises a bit-interleaved scheme, as described in the previous section.

Fig. 6 shows the bit-line swing simulation results with the proposed 10T bit cell in a 300 mV power supply and typical process corner. In this simulation, we measured the bit-line swing at steady-state after word-line was enabled in read mode. According to the result, the cell numbers per bit-line affect the bit-line voltage swing and bit-line loading. This study proposes 64 cells per bit-line to decrease bit-line loading; however, the bit-line swing was in the acceptable range. The proposed subthreshold SRAM was composed of 16 blocks, and each block had 4 columns, which shared a virtual ground driver. The block architecture is shown in Fig .5.

TABLE Ⅱ. COMPARISON OF RESULT

	[1]	[3]	[4]	[5]	[7]	This Work
Technology	65nm CMOS	130nm CMOS	130nm CMOS	90nm CMOS	90nm CMOS	**90nm CMOS**
Density	256kb	480kb	512x13	4kb	4kb	**4kb**
Cell number per BL	256	1k	16	256	256	**64**
Cell type	10T	10T	7T	8T	8T	**10T**
VDD min	0.32V	0.2V	0.19V	0.2V	0.38V	**0.3V**
Performance	465kHz @0.4V	120 kHz @ 0.2V	28 kHz @ 0.19V	6MHz @0.2V	6MHz @0.38V	**10MHz @0.3V**
Power consumption	3.28 µW	2.04 µW	1.197 µW @0.31V	10.4 µW	2.99 µW	**4.25µW**
One read/write operation energy	14.1pJ	34pJ	N/A*	3.47pJ	0.998pJ	**0.85pJ**

N/A*: The voltage of performance differs from the voltage of power consumption. Thus, it cannot calculate the operational energy.

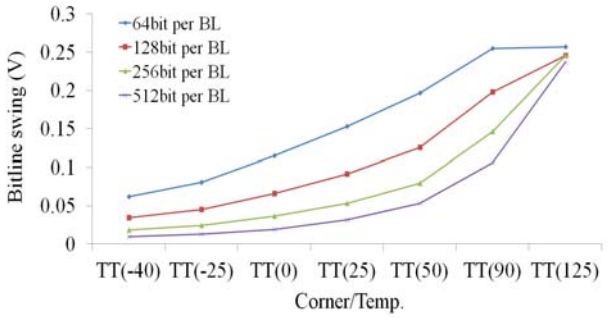

Figure 6. Analysis result of bit-line swing (with 300 mV power supply in typical process corner) at steady-state after WL enable

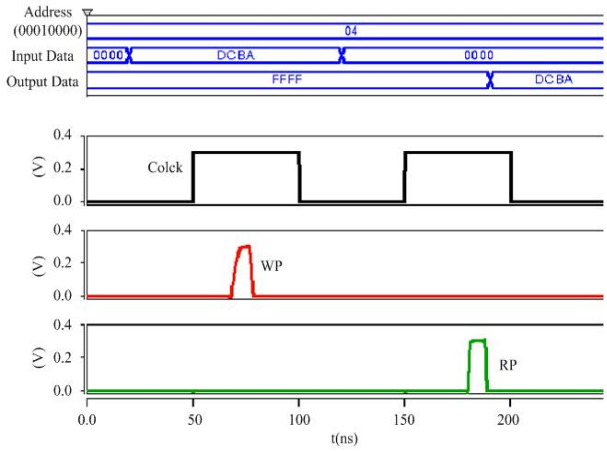

Figure 7. The simulation result of write data ”DCBA” and read data “DCBA”

The address decoder in SRAMs is a device that provides 4 n-bit addresses to select the signal for WWL_A, WWL_B, WWL_C, and WWL_D. Because row decoders have 6-bits, they must use 6 input AND gates; however, the gate delay increases because of an excessive number of fans in a single logic gate. Gate delay is more obvious in the subthreshold. Therefore, we propose a two-stage decoder (4x3) to decrease gate delay. The average power of the address decoder in this study was 0.377 µW.

For the proposed SRAM, the signal generator produced a write pulse (WP), read pulse (RP), precharge signal, and enable pulse (EN). Write pulse is used to control write circuit. Read pulse was used to control the virtual ground. The EN controls the transmission gate of each BL and sense amplifiers, it is only generated after the read pulse.

V. CONCLUSION

This study implemented a 4kb 10T subthreshold SRAM in a 90 nm CMOS technology with a differential read scheme and bit-interleaving scheme. High Vth NMOS was used to reduce bit-line leakage to decrease power consumption. We simulated the 4kb SRAM operation with a normal Vth NMOS in the path of write with power consumption of 9.05 µW; with high Vth NMOS, the power consumption decreased to 4.25 µW. The simulation results showed that an operation frequency of 10 MHz at 300 mV was achieved, as shown in Fig. 7 The average power consumption was 4.25 µW and energy consumption was 0.85 pJ at 10 MHz and 300 mV. The standby power consumption was 2.26 µW. Table Ⅱ shows a comparison of the results with a number of recently reported SRAMs.

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REFERENCES

[1] B. H. Calhoun, A. P. Chandrakasan, “A 256-kb 65-nm Sub-threshold SRAM Design for Ultra-Low-Voltage Operation” *IEEE J. Solid-State Circuits*, vol. 42, no. 3, pp.680–688, Mar, 2007

[2] Ik Joon Chang, Jae-Joon Kim, Sang Phill Park, Student Member, IEEE, and Kaushik Roy, " A 32 kb 10T Sub-Threshold SRAM Array With Bit-Interleaving and Differential Read Scheme in 90 nm CMOS" *IEEE J. Solid-State Circuits*, vol. 44,no.2, pp. 650 – 658, Feb. 2009

[3] Tae-Hyoung Kim, Liu J, Keane J, Kim C.H.," A 0.2 V, 480 kb Subthreshold SRAM With 1 k Cells Per Bitline for Ultra-Low-Voltage Computing" *IEEE J. Solid-State Circuits*, vol. 43, no. 2, pp.518–529, Feb, 2008

[4] J. Chen, L. T. Clark, and T. Chen,"An ultra-low-power memory with a Subthreshold power supply voltage," *IEEE J. Solid-State Circuits*, vol.41, no. 10, pp. 2344–2353, Oct. 2006

[5] M. H. Tu, J. Y. Lin, M. C. Tsai, S. J. Jou, C. T. Chuang, "Single-Ended Subthreshold SRAM with Asymmetrical Write/Read-Assist," *IEEE Transactions on CAS-I*, Vol.57, No.12, pp.3039-3047, Dec. 2010

[6] R. Singh and N. Baht, "An offset compensation technique for latch type sense amplifiers in high-speed low-power SRAMs," *IEEE Trans. VLSI Syst. Trans. Briefs*, vol. 12, no. 6, pp. 652–657, Jun. 2004

[7] Yi-Wei Chiu, Jihi-Yu Lin, Ming-Hsien Tu, Shyh-Jye Jou and Ching-Te Chuang, "8T Single-ended Sub-threshold SRAM with Cross-Point Data-aware Write Operation" *Low Power Electronics and Design (ISLPED)*, Aug , 2011 , pp.169-174

[8] Ming-Hung Chang, Yi-Te Chiu, Shu-Lin Lai, and Wei Hwang, " A 1kb 9T Subthreshold SRAM with Bit-interleaving Scheme in 65nm CMOS", *Low Power Electronics and Design (ISLPED)*, Aug, 2011, pp. 291 – 296

[9] P. Hazucha et al., "Neutron soft error rate measurements in 90-nm CMOS process and scaling trends from 0.25-µm to 90-nm generation," in *IEDM Tech. Dig*., Dec. 2003, pp. 21.5.1–21.5.4

[10] R. Baumann, "The impact of technology scaling on soft error rate performance and limits to the efficacy of error correction," *IEEE Int'l Electron Devices Meeting*, Feb. 2003, pp. 329-332

[11] I. Carlson, S. Andersson, S. Natarajan, and A. Alvandpour, "A high density, low leakage, 5T SRAM for embedded caches," in *Proc. 30th European Solid State Circuits Conf. (ESSCIRC)*, Sep. 2004, pp. 215–218

[12] R. Aly, M. Faisal, and A. Bayoumi, "Novel 7T SRAM cell for low power cache design," in *Proc. IEEE SOC Conf*., Sept. 2005, pp. 171–174

[13] Selimis, G. Konijnenburg, M. ; Ashouei, M. ; Huisken, J. ; de Groot, H. ; van der Leest, V. ; Schrijen, G.-J. ; van Hulst, M. ; Tuyls, P. " Evaluation of 90nm 6T-SRAM as Physical Unclonable Function for secure key generation in wireless sensor nodes", *Circuits and Systems (ISCAS), IEEE International Symposium*, May, 2011 , pp. 567–570