CMOS Magnetic Field to Frequency Converter

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***Abstract*—In this paper, a CMOS magnetic field to frequency converter with high resolution is presented. It is composed of two voltage-controlled ring oscillators whose output frequency differences linearly vary with the magnetic field perpendicular to the chip surface. The prototype circuit has been fabricated in a 0.5-μm CMOS process and operated at a 5-V supply voltage. The measured sensitivity is 24 kHz/mT and the power consumption is 5.1 mW. The small equivalent resolution of at least 20 μT can be achieved. The frequency offset is 42 kHz when no magnetic field applied. Its nonlinearity within $\pm$120 mT is smaller than 0.56%.**

***Index Terms*—C^{2}MOS, Magnetic MOSFET (MAGFET), magnetooperational amplifier (MOP), magnetically controlled oscillator (MCO).**

I. Introduction

A MAGNETIC sensor is a transducer which can convert a magnetic field into a corresponding electrical signal. There are a lot of industrial applications where magnetic sensors can be found [1], [2], such as brushless motor controls, current measurement, monitoring the exposure to magnetic field [3], automotive applications, etc. Integrated microsensors with on-chip interface circuits are currently replacing discrete sensors in view of their inherent advantages, such as low cost, high reliability, and on-chip processing capability. The output signal of a sensor can be converted into different forms depending on the circuit approaches used and system applications. To achieve small, robust, and low-cost micro systems, it is desirable to integrate the magnetic sensor with analog signal conditioning circuits so that their output can be fully compatible with digital signal processors. In this paper, a highly sensitive magnetic field sensor with frequency output is presented by using the magnetic MOSFET (MAGFET) [4] in a standard CMOS process. In this work, we integrate the magnetooperational amplifier (MOP) [5], [6] with two voltage-controlled ring oscillators to realize the magnetic field sensor.

This paper is organized as follows. In Section II, the magnetic field detection by the MOP is reviewed. Then, the magnetically-controlled delay element and the magnetically voltage-controlled ring oscillator will be described. In Section III, the experimental results are given, and the conclusion is given in Section IV.

Manuscript received March 25, 2002; revised October 31, 2002. The associate editor coordinating the review of this paper and approving it for publication was Dr. Andre Bossche.

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Digital Object Identifier 10.1109/JSEN.2002.807485

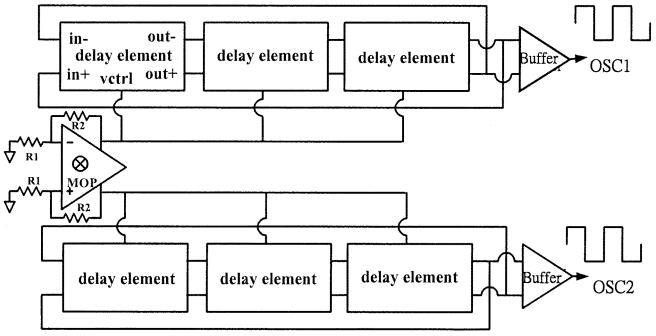

Fig. 1. Proposed magnetic sensor with frequency output.

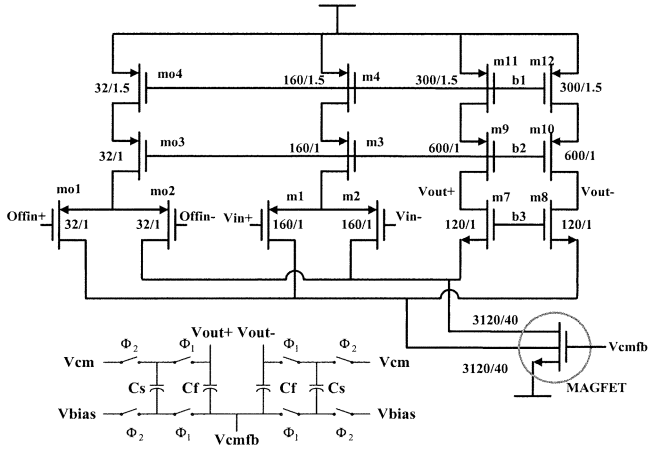

Fig. 2. Proposed CMOS magneto-operational amplifier.

II. Circuit Description

The proposed magnetic field sensor is shown in Fig. 1. It is composed of the CMOS MOP [5], [6] and two voltage-controlled ring oscillators, which are controlled by the MOP. The schematic of the MOP with the switched-capacitor common mode feedback circuit is shown in Fig. 2. The MOP is a conventional folded-cascode amplifier except that the NMOS current sources are replaced by MAGFET arrays. Taking the layout mismatch problem and optimal sensitivity into account simultaneously, we choose the n channel MAGFET as the sensing element and the aspect ratio of each MAGFET device in the following sections is chosen to be $W/L = 80$ μm/40 μm and $d = 2$, according to [6]. Since the bias current of the MAGFET is 700 μA, the power consumption of this chip mainly comes from the MOP. When no magnetic field is applied, the output drain currents of MAGFET are equal, which means that the voltage difference between the two differential outputs of the MOP is zero. In this situation, the MOP works just like a general operational amplifier. The additional differential pair, mo1 and mo2 in Fig. 2, is used to null the offset voltage. When the perpendicular

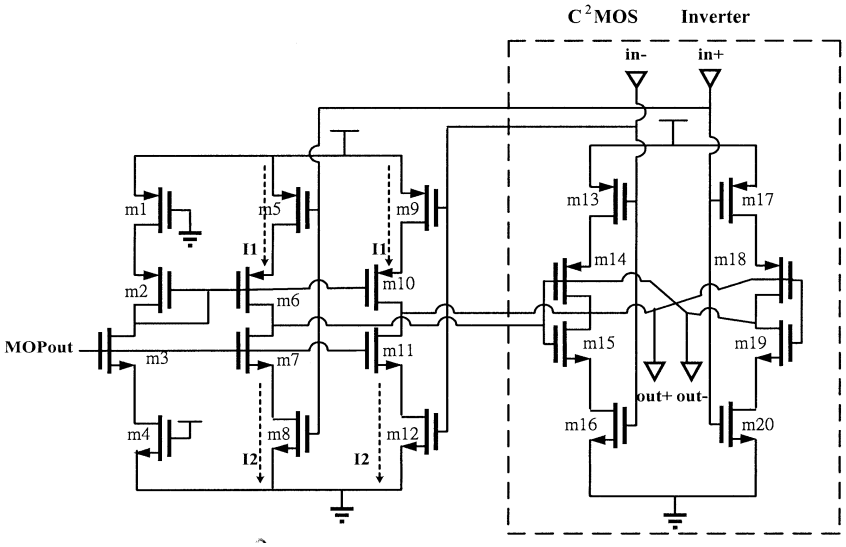

Fig. 3. Delay element.

magnetic field is applied, there is a current imbalance between these two drains. The voltage difference between the differential outputs $V_{\text{out}+}$ and $V_{\text{out}-}$ will be generated. One can assume that a magnetic field induced voltage is added to the input of the MOP. So, the output voltage of the MOP can be expressed as

$$V_{\text{out}+} - V_{\text{out}-} = A \cdot (V_{\text{in}+} - V_{\text{in}-} + v_m) \tag{1}$$

where A is the finite dc gain of this operational amplifier and $v_m (= S_m \cdot B_\perp)$ is the induced voltage. The conversion gain S_m denotes the ratio between the induced voltage v_m and the perpendicular magnetic field $B_\perp$. By connecting the MOP with resistors into an inverting amplifier, the linearity could be improved and the gain and sensitivity could be adjusted by the resistive ratio.

The voltage-controlled ring oscillator is composed of the magnetically controlled delay elements. This delay element is shown in Fig. 3 and it consists of two clocked CMOS (C^2MOS) inverters [7], [8] with four switches (m6, m7, m10, and m11) and four current sources (m5, m8, m9, and m12), which are generated by the outputs of the MOP. Two C^2MOS inverters are interconnected to speed up the transition for the output swing between $V_{DD} - V_{TP}$ and V_{TN}, where V_{DD} is the supply voltage and V_{TP} and V_{TN} are the threshold voltages of PMOS and NMOS transistors, respectively. Transistors, m1 and m4, are added to match the current sources with switches. The current source I_2 can be expressed as

$$I_2 = K\left(V_{GS0} + r \cdot S_m \cdot B_\perp - V_{TN}\right)^2 \tag{2}$$

where K is the transcoductance parameter, V_{GS0} is the original overdrive of the transistor driven by the MOP when no external magnetic field is applied, and $r (\equiv 1 + (R_2/R_1))$ is the voltage gain as shown in Fig. 1. The operation of the delay element can be described as follows [8].

If the In+ increases to V_{DD} and in− decreases to ground, m8 is turned on (m5 is turned off) and the current I_2 from m7 discharges out−; meanwhile, m9 is turned on (m12 is turned off) and the current I_1 from m10 charges out+. In the beginning, out− is pulled down slowly by I_2, and m14 would not been turned on until out− is lower than $V_{DD} - V_{TP}$. Then, out+ will be charged to V_{DD} quickly due the positive feedback of the C^2MOS latch. In the same way, out+ increases slowly at first, and m20 would not be turned on until out+ increased higher than V_{TN}. Then, out+ will be discharged to ground quickly. The controlled current I_2 is used to discharge the output node from V_{DD} to $V_{DD} - V_{TP}$. If the state transition time for this C^2MOS latch can be neglected, the delay time T_D of this delay element can be expressed as

$$T_D \approx \frac{C \times V_{TP}}{I_2} \tag{3}$$

where C is the capacitive load of the output node. Two current sources I_1 are used to compensate the clock feed-through coupling because this clock feed-through would result in the distortion of the duty cycle [8]. In summary, this delay time of the delay element should mainly be contributed from T_D and the time spending on the state transition in the regenerative latch could be neglected compared to T_D. The delay cell can provide wide delay range and negligible dc power dissipation.

The number of stages in a ring oscillator can be determined by various requirements, including speed, power dissipation, noise immunity, etc. By cascading odd N delay elements in a loop, a ring oscillator can be formed; and its oscillating frequency can be given as

$$f_{OSC} = \frac{1}{N \times T_D} \tag{4}$$

where T_D is the delay time of each delay element. We choose $N = 3$ for compromise among power, speed and chip area.

However, the output frequency shown in (4) is a square term rather than a linear term related to $B_\perp$. To compensate the nonlinearity appear in (4), two ring oscillators are connected with the MOP in a fully differential manner as shown in Fig. 1. One can obtain the difference of the output frequencies by frequency counters to obtain a linear term. This structure has two advantages. One is that the sensitivity is doubled. The other is that the

Fig. 4. Die photo of the proposed magnetic sensor.

even-order nonlinear terms can be cancelled if these two ring oscillators are well matched. The output frequency difference can be expressed as

$$\Delta f = f_{OSC1} - f_{OSC2} = \frac{4K \cdot r \cdot S_m \cdot B_\perp}{N \cdot C \cdot V_{TP}} \cdot (V_{GS0} - V_{TN}). \quad (5)$$

From (5), the frequency difference relative to B can be maximized by adjusting various variables such as N, C, r, and V_{GS0}. The fully differential structure of the MOP and the ring oscillators can not only increase the sensitivity, but also minimize some sensor defects like offset and nonlinearity. Moreover, the MOP increases the sensitivity of the MAGFET device by the factor of the feedback resistor ratio, and the MOP is integrated with the ring oscillators to produce a frequency-modulated signal which is highly immune to noise and interferences.

III. Experimental Results and Discussions

The sensor has been fabricated in a 0.5-μm CMOS technology with a 5-V supply voltage. The die photo of the proposed magnetic field to frequency converter is shown in Fig. 4, and the total area is 1.38 mm * 1 mm excluding the I/O pads. The off-chip feedback resistors for the MOP is $R_1 = 1$ kΩ and $R_2 = 220$ kΩ, respectively. The buffers of the oscillators are two inverters made on chip for driving the external load. The magnetic field perpendicular to the chip is generated by an electromagnet core which is powered by the GW regulated dc power supply (Model GPR-22H10H). The current supplied by this power supply controls the magnitude and polarity of the generated field. The generated field is checked by the Gauss/Tesla meter (F.W. BELL model 5080) with a Hall probe closely approximating to the test chip. The above mentioned equipment and devices are caged in an iron shell. Although this cannot shield the Earth's magnetic field from introducing offset frequency, it can prevent other electric effects from the air as completely as possible. The remedy for the offset induced by the Earth itself is to shield the Hall probe in the zero flux chamber of Gauss/Tesla meter before our measurement stage. The output frequency of the magnetically controlled oscillator (MCO) was studied as a function of the dc magnetic induction, and these two output signals from two oscillators are connected to the frequency counter to fulfill the subtraction.

The measured output frequency differences are shown in Figs. 5 and 6. Each measured data is obtained by averaging five measurements. The coarse measurement result is plotted in

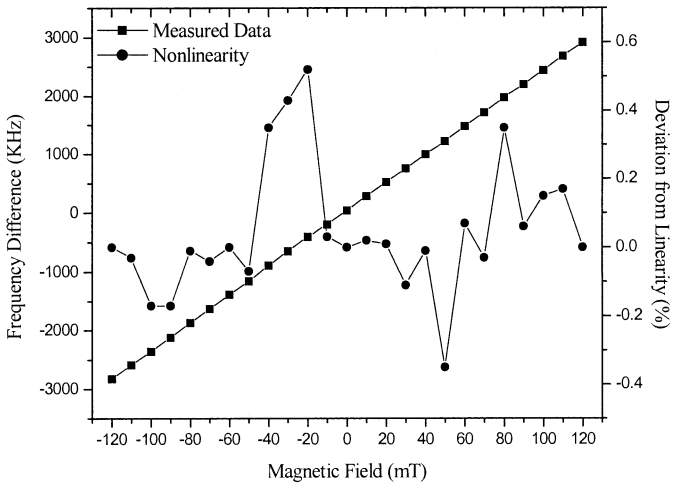

Fig. 5. Coarse measurement result.

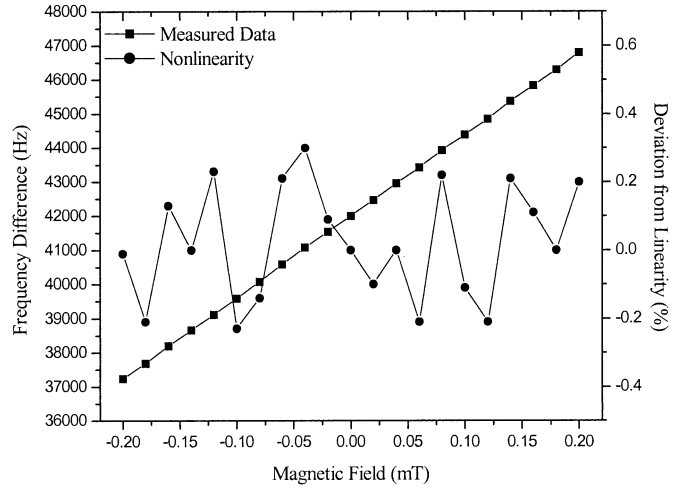

Fig. 6. Fine measurement result.

TABLE I
Performance Summary of the Proposed Magnetic Field to Frequency Converter

Range	±120 mT
Offset frequency	42 kHz
Resolution	< 20 uT
Sensitivity (kHz/mT)	27 (simulation) 24(measurement)

Fig. 5, where the range is within ±120 mT and the magnitude incremental is 10 mT. From this plot, the linear response owing to the magnetic field can be obtained. The calculated sensitivity is 24 kHz/mT. Fig. 6 shows the resolution test. The linearity is also maintained in this range of ±0.2 mT with 20 μT increment. From this plot, we can deduce that the real resolution should be much smaller. Restricted by the accuracy of the instruments, the change of the magnetic filed smaller than 20 μT could not be generated for further verifications. Since only the dc magnetic field signal is tested, the cut off frequency for the magnetic

TABLE II
PERFORMANCE COMPARISONS WITH PUBLISHED WORKS

	Proposed	[10]	[11]	[12]	[13]
Range (mT)	±120mT	±400mT	±1000mT	0~10mT	0.2-2.6mT
Sensitivity(Hz/mT)	24015	200	0.184	3	79
Linearity	0.56%	0.1%	0.1%	10%	5.6%
Resolution	< 20 uT	<5 mT	Not mentioned	100 uT	400 uT
VDD	5V	1V	10V	2V	5V
Power	5.1mW	1.2mW	6.2mW	0.2uW	135uW
Figure of Merit= $\frac{sensitivity(Hz/mT)}{power(mW)\bullet linearity(\%)}$	8408.6	1666.7	0.3	1500	104.5
Process	0.5um CMOS	N-type wafer	5um CMOS	2.5um CMOS	Not mentioned

signal should be low. The minimum detectable magnetic field of the proposed circuit under dc excitation is limited by $1/f$ noise and not by thermal noise.

In Fig. 6, the output frequency with no magnetic field corresponds to the center frequency of 42 kHz. This offset phenomenon can be caused from mismatch from the MOP and any mismatch between these two oscillators. The performance summary is given in Table I. This sensor's nonlinearity is less than 0.56% for the magnetic field within ± 120 mT. The power consumption of the proposed magnetic sensor is 5.1 mW. The measured sensitivity (24 kHz/mT) shows the degradation compared with the simulation result (27 kHz/mT). The nonlinearity problem may be caused by any mismatch between the differential paths and temperature effects. For example, there is a mismatch between the resistors R1 and R2 in the MOP or mismatch in the output capacitances of the delay elements, and the even order nonlinear terms can not be completely cancelled like in (5).

The temperature characteristics of the chip are verified from HSPICE simulations. The temperature impact on output frequency variations is examined under different process corner variations and different frequencies. The largest frequency variations are 8.32% under four different process corners and 8.57% during the range of 20–40 °C. These values correspond approximately to 5000 ppm/°C and agree exactly with that of MAGFET reported ain [9].

Performance comparisons with published works using MAGFETs are listed in Table II. Our work can give the improvement in sensitivity over previously reported works using MAGFETs. Moreover, a figure of merit is defined as $(sensitivity(\text{Hz/mT}))/(power(\text{mW}) \bullet linearity(\%))$ and our work can achieve the best figure of merit in Table II.

IV. CONCLUSION

A highly sensitive magnetic field sensor with the sensitivity of 24 KHz/mT is presented. This sensor can detect the magnetic fields smaller than 20 μT. Compared with the published works with frequency output by using MAGFETs, it can exhibit a good figure of merit and the fine resolution according to Table II. The frequency output can be further processed by digital signal processing circuits, such as a microcontroller, to achieve the high resolutions.

ACKNOWLEDGMENT

The authors would like to thank the Chip Implementation Center (CIC) of the National Science Council, Taiwan, R.O.C., for fabricating the chips.

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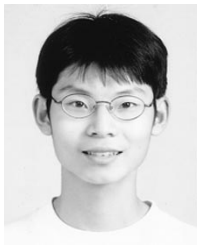

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