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Yi-Ju Chen, Cheng-Huang Kuo[1], Chun-Ju Tun[1], Shih-Chieh Hsu[2], Yuh-Jen Cheng[2], and Cheng-Yi Liu*

Department of Chemical and Materials Engineering, National Central University, No. 300, Jhongda Rd., Jhongli, Taoyuan 32001, Taiwan, R.O.C.
[1]*Department of Optics and Photonics, National Central University, No. 300, Jhongda Rd., Jhongli, Taoyuan 32001, Taiwan, R.O.C.*
[2]*Research Center for Applied Sciences, Academia Sinica, 128 Academia Road, Section 2, Nankang, Taipei 115, Taiwan, R.O.C.*

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A pyramidal pattern was produced on a *c*-plane sapphire substrate by a mask-free etching process. Photoluminescence (PL) results show that a GaN-based light-emitting diode (LED) epilayer grown on the pyramidally patterned sapphire substrate has higher epitaxial quality than that grown on a standard flat *c*-plane sapphire substrate. When the input current is 350 mA, the average light output power of LED chips on the pyramidally patterned sapphire substrate is 37% larger than that of LED chips on a standard *c*-plane sapphire substrate.

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In recent years, GaN-based light-emitting diode (LED) have been widely recognized to be the most promising alternative light source for general lighting.[1,2] Using the break through patterned sapphire substrate technique, Nichia Corporation has achieved high-brightness GaN-based LEDs with a record-high efficiency of 150 lm/W.[3,4] The enhancement in efficiency of GaN-based LEDs on patterned sapphire substrates is generally attributed to the improvement in both light extraction efficiency and internal quantum efficiency.[5–9] The improvement in internal quantum efficiency is due to the reduction in threading dislocation density by the achievement of lateral growth of a GaN epilayer on the patterned sapphire substrate.[10–13] The light extraction efficiency is enhanced by the regular pattern created on the sapphire substrate, which counteracts the effect of total internal reflection (TIR) at the GaN/sapphire interface.[5]

Numerous patterning features produced on patterned sapphire substrates by either dry etching or wet etching processes, which include circular cavities, square cavities, hemispherical bumps, and trenched stripes, have been studied.[5,14–17] However, no matter what etching process is used to create the patterns, a hard-mask (SiO_2 in most cases) lithographic process is required on the flat *c*-plane sapphire wafer. In this study, we utilize a mask-free wet-etching process to produce a so-called nature-patterned sapphire substrate (n-pss), with a unique pyramidal pattern on the *c*-plane sapphire surface. In addition, metal organic chemical vapor deposition (MOCVD) is used to grow a GaN epitaxial layer with an LED structure on the n-pss wafer. The optical and electrical properties of horizontal LED chips fabricated on the n-pss wafer are characterized in detail.

The mask-free wet-etching process used to produce the pyramidal n-pss wafers is described in detail in the following. Before the wet etching process, a SiO_2 layer was deposited by plasma-enhanced chemical vapor deposition (PECVD) on the back side of the *c*-plane sapphire wafer to prevent the back side from being etched. The flat back side of the patterned sapphire wafer also enables good contact with the bottom of the growth pot in the MOCVD chamber, which ensures the high quality of the MOCVD epitaxial process. After deposition of the SiO_2 back side layer, the sapphire wafer was immersed in pure H_2SO_4. The etching temperature was controlled at a constant temperature of 320 °C for periods of 15, 30, and 60 min. After etching, dilute HF solution was used to remove the SiO_2 back-side layer. Finally, the etched sapphire wafer was successively cleaned by acetone, isopropyl alcohol (IPA), and distilled water (DI water).

We found that H_2SO_4 did not significantly etch the sapphire wafer in the thickness direction. Instead, it was found that a massive cubic etching product phase completely covered the surface of the sapphire wafer, as shown in Fig. 1(a). X-ray diffraction (XRD) was used to identify the exact compound phase of the etching-product. As shown in Fig. 1(b), only one strong peak appears in the XRD diffraction pattern, which matches the standard XRD diffraction pattern of the $Al_2(SO_4)_3 \cdot 17H_2O$ phase. Dwikusuma *et al.* also reported similar findings, i.e., the formation of the $Al_2(SO_4)_3 \cdot 17H_2O$ phase on sapphire etched by H_2SO_4.[18] However, Dwikusuma *et al.*'s XRD result showed all the diffraction peaks of the $Al_2(SO_4)_3 \cdot 17H_2O$ phase but in the present study, the $Al_2(SO_4)_3 \cdot 17H_2O$ etching product exhibits an orientation-preferred XRD diffraction pattern. Faceted pyramids were observed on the n-pss wafers after removal of the etching product in dilute HCl solution. Figure 1(c) shows an enlarged scanning electron microscope (SEM) image of the facet pyramids on the n-pss wafer surface. We found the size of the pyramids on the n-pss wafer to be reasonably uniform, the height and width of the pyramids being about 0.2 and 1.5 μm, respectively. In addition, a flat *c*-plane sapphire surface appears between the pyramids. This flat *c*-plane sapphire surface is of importance since it can provide suitable nucleation sites for the initial growth of the buffer GaN epilayer on the patterned sapphire substrate. The average coverage percentage of the pyramids on the etched sapphire wafer is about 44%. Note that patterns typically cover about 50 to 70% of patterned sapphire substrates.[5,15,17] In other words, the percentage coverage of the currently studied pyramidal pattern on the etched sapphire wafer is less than the typical coverage.

Energy-dispersive spectrometry (EDS) analysis of the pyramids produce no signal indicative of S atoms; Al and O are the only two elements that can be detected (the atomic ratio of Al to O is about 2 : 3). Therefore, we believe that the etching-product phase covering the sapphire surface was

*E-mail address: chengyi@cc.ncu.edu.tw

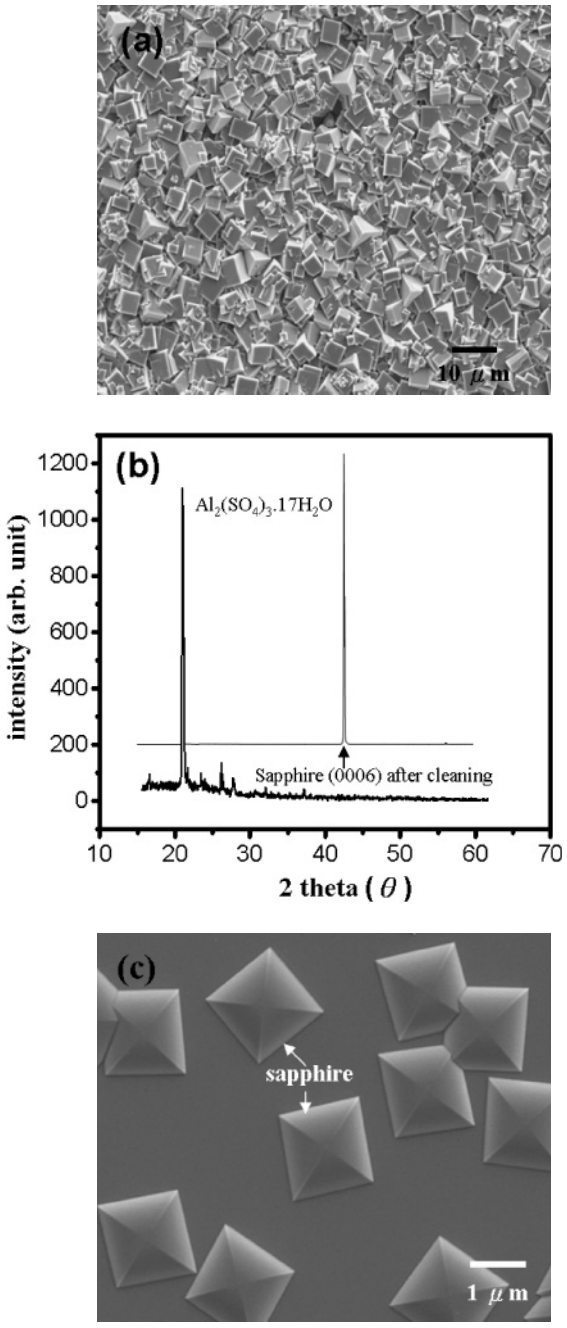

Fig. 1. (a) Etching-product layer on the etched sapphire surface; (b) diffraction pattern of the $Al_2(SO_4)_3 \cdot 17H_2O$ phase; (c) enlarged SEM image of the facet pyramids on the n-pss wafer surface.

completely removed by the HCl solution. Glancing XRD was also performed on the pyramids on the n-pss surface. The glancing XRD diffraction pattern further confirms that the phase of the pyramids on the sapphire wafer was the pure sapphire phase (not the etching-product).

Figure 2(a) shows a tilted SEM view of the pyramids on the n-pss wafer. We can clearly see that the four side planes of the pyramid are not flat. The curve of the side planes of the pyramids, reminiscent of an upper convex meniscus, was produced in response to the flat *c*-plane surface. Figure 2(b) shows a focused ion beam (FIB) cross-sectional image of a single pyramid on the n-pss wafer surface. The dihedral angle of the side planes of the pyramid (relative to the *c*-plane sapphire) decreases with the height of the pyramid.

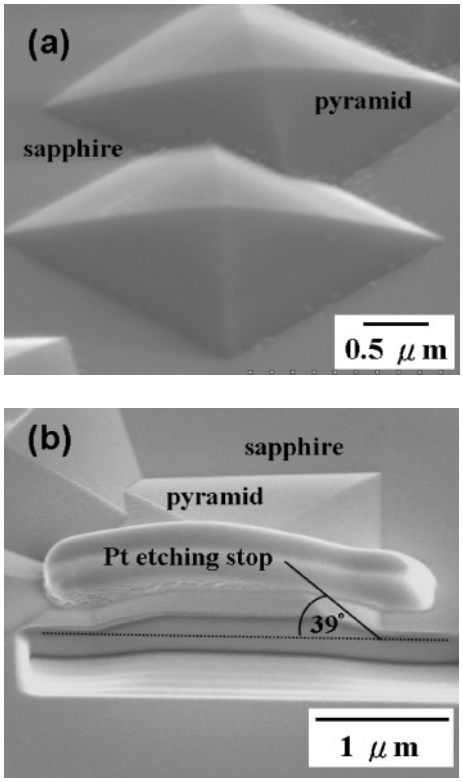

Fig. 2. (a) Tilted SEM view of the pyramids; (b) FIB cross-sectional image of a pyramid.

The dihedral angle at the bottom of the pyramid was estimated from the FIB cross-sectional image to be about 39°. The dihedral angle of the side planes with respect to the *c*-planes at the top of the pyramids was as low as 10°. Thus, we believe that the side planes of the pyramids were not common sapphire planes, such as r, m, or a planes, but were composed of many high-index planes.

This novel pyramidal pattern on the n-pss wafer was considered to have similar functions to other patterns reported to be formed on sapphires, which allow a marked improvement in external quantum efficiency.[5–9] This is why it is of interest to grow epitaxial GaN/InGaN LED structures on pyramidally patterned n-pss wafers by MOCVD. The LED epitaxial structure includes a 1.8-μm-thick undoped GaN layer and a 2.5-μm-thick Si-doped n-type GaN cladding layer, an active region emitting light with a 450 nm wavelength with six periods of InGaN/GaN multiple quantum wells (MQWs), and a 0.3-μm-thick Mg-doped p-type GaN cladding layer. Figure 3 shows the results of PL measurement of the GaN epilayer grown on the n-pss wafer and the standard *c*-plane sapphire wafer. PL measurement of the GaN epilayer on the n-pss wafer indicates a higher intensity and narrower full width at half maximum (FWHM) than those of the GaN epilayer grown on the standard sapphire wafer. This is indicative of the higher axial quality of the GaN epilayer grown on the n-pss wafer (i.e., lower defect level) than that of the GaN epilayer grown on the standard *c*-plane sapphire wafer.

GaN LED epilayers grown on the n-pss wafer and the standard sapphire wafer were fabricated into horizontal LED chips with dimensions of $1 \times 1\,mm^2$. The luminous–input current–voltage (*L–I–V*) curves of LED chips on the n-pss

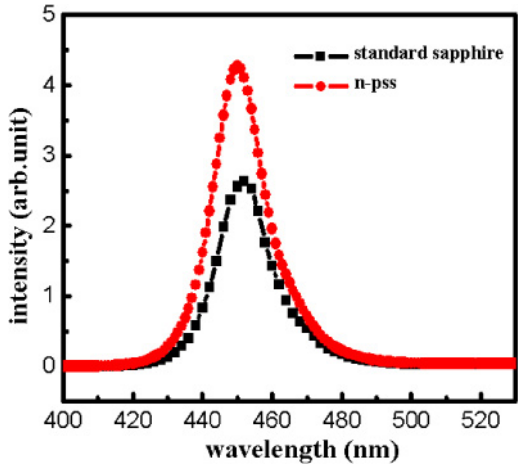

Fig. 3. (Color online) PL measurements of the GaN epilayer grown on the n-pss wafer and the standard *c*-plane sapphire wafer.

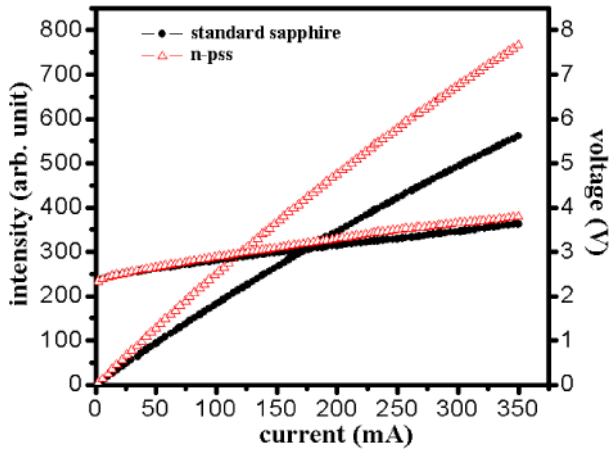

Fig. 4. (Color online) *L–I–V* curves of LED chips on the n-pss wafer and the standard sapphire wafer.

wafer and the standard sapphire wafer are plotted in Fig. 4. When the input current is 350 mA, the turn-on voltages of both LED chips are similar (about 3.6 V). The leakage currents for the LED chips on the standard sapphire wafer and n-pss sapphire wafer are -1.7×10^{-7} and -9.5×10^{-7} at -5 V, respectively. The above results indicate that the electrical performance of LED chips fabricated on the n-pss and standard sapphire wafers is very similar. From the *L–I* curve (measured by an integral sphere apparatus), it was revealed that the LED chips on the n-pss wafer have a higher light output power than those on the standard sapphire wafer. At an input current of 350 mA, the average light output power of the LED chips on the n-pss wafer is 37% larger than that of the LED chips on the standard sapphire wafer.

In conclusion, a pyramidal pattern was created on a *c*-plane sapphire substrate by a mask-free etching process. The PL results show that a GaN LED epilayer can be successfully grown on the pyramidal sapphire surface, which has higher crystalline quality than a GaN epilayer grown on a standard flat sapphire. For an input current of 350 mA, the average light output power of LED chips on the pyramidally patterned sapphire substrate is 37% larger than that of LED chips on a standard *c*-plane sapphire substrate. We believe the pyramidal structure on the sapphire to be the key to greatly enhancing the light extraction efficiency and external quantum efficiency of LED chips.

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