Cascaded Feedforward Sigma-delta Modulator for Wide Bandwidth Applications

Jen-Shiun Chiang, Teng-Hung Chang and Pou-Chu Chou

Department of Electrical Engineering
Tamkang University
Tamsui, Taipei, Taiwan 251, R.O.C.
E-mail: chiang@ee.tku.edu.tw

Abstract

A new sigma-delta modulator architecture for wide bandwidth application called cascaded feedforward sigma-delta modulator is proposed in this paper. This sigma-delta modulator is similar to the conventional feedforward summation sigma-delta modulator. The conventional feedforward summation sigma-delta modulator uses multi-bit feedback and therefore a multi-bit digital-to-analog converter (DAC) is needed. Due to the nonlinearity of the multi-bit DAC, it is difficult to be implemented. On the other hand the proposed approach uses 1.5-bit feedback, and thus the implementation of the analog part is much easier than the conventional one. Since the 1.5-bit feedback will cause coarse quantization errors, error cancellation must be done in the digital part. Here an adaptive filter with least mean square algorithm is used to reduce the nonlinear effect. The simulation results show that the signal to noise plus distortion ratio (SNDR) of this architecture is very close to that of the ideal feedforward summation sigma-delta modulator with multi-bit DAC and can be used for the wide bandwidth application.

***Key Words*:** Wide-bandwidth, Cascaded Sigma-delta Modulator, Feedforward, xDSL, Dual-quantizer

1. Introduction

The sigma-delta modulation (SDM) technique has become popular in the design of high-performance analog-to-digital converters [1]. Due to the oversampling approach, SDM is difficult to be implemented in the wide bandwidth applications, such as image processing, wideband CDMA, …, etc. There are many varieties of architectures to design a sigma-delta modulation such as MASH, single-loop, cascaded, feedforward summation, distributed feedback, …, etc [8]. The feedforward summation with local resonator feedback sigma-delta modulator (FFSDM) [8] is realized by using analog filter design approach and is suitable for wide-bandwidth applications. In FFSDM, it is implemented by analog filter design approach, and thus the cut-off frequency (3dB frequency) can be easily decided to determine the desired bandwidth and noise floor. Kuo et al. proposed a high order FFSDM synthesis tool (HOST) to decide the filter coefficients and make the realization of FFSDM very easily [7]. In order to be applied to the wide-bandwidth systems in FFSDM, multi-bit quantization is used for achieving the desired signal-to-noise ratio (SNR). For a fixed order SDM, we can increase the bit numbers of the internal quantizer or the oversampling ratio (OSR) to improve the SNR. Due to the oversampling nature, in wide bandwidth applications the OSR of a SDM cannot be very high otherwise the bandwidth will be very limited. Therefore, in the wide bandwidth SDM design we have to increase the bit numbers of the internal quantizer instead of OSR to gainenough SNR. For that reason, a multi-bit digital-to-analog converter

(DAC) in the feedback of the SDM is required. As we know, in the VLSI circuit design the DAC has the inherent nonlinearity, and may cause design complication significantly. In order to make the SDM implementation easier, we propose a new SDM architecture that is similar to the architecture of FFSDM but without multi-bit DAC; we call this SDM as cascaded feedforward sigma-delta modulator (CFFSDM). In this architecture, a 1.5-bit quantizer substitutes the multi-bit DAC, and the error cancellation technique is adopted to eliminate the coarse quantization error in the digital part. Generally, digital circuits have better linearity than analog circuits (DAC). Since the technology of digital circuits is very matured currently, and the implementation of the analog circuits of CFFSDM is not difficult, all these characteristics show that this new SDM can be easily implemented to a wide bandwidth application.

This paper is organized as follows: Section 1 is the introduction. Section 2 describes the conventional wide-bandwidth SDM architecture. Section 3 illustrates the architecture of CFFSDM. We analyze the non-ideal effects of CFFSDM in Section 4; the comparisons and simulation results are shown in Section 5. Finally we give the conclusion in Section 6.

2. Architectures of the Conventional Wide Bandwidth Sigma-Delta ADC

The sigma-delta analog to digital conversion has been popular over the past 15 years. It exploits the advancing of the modern fine-line CMOS process to obtain high-resolution ADC without suffering from its inaccuracy. However, due to its oversampling nature, the conversion bandwidth of the sigma-delta ADC is severely limited. This limitation can be partly alleviated by using some special architecture such as cascaded multistage architecture or MASH [10]. MASH combines several low order modulators to achieve a high-order noise shaping function, and can improve the performance by increasing stages or orders. However, the mismatch between stages may degrade the performance. In order to maintain a good performance for a cascaded SDM with one bit quantizer, it has to increase the OSR or order. Another approach to improve SNR is to use multi-bit quantizer [5]. For example, the SNR of a second order cascaded SDM can be obtained by the following equation [8]:

$$SNR_{\max} = 6.02N + 1.76 - 12.9 + 50\log(OSR) \quad (1)$$

where N is the bit number of the quantization. From equation (1), we can find that doubling the OSR improves the SNR by 15 dB and increasing 1 bit of the quantization can improve the SNR by 6 dB.

The noise transfer function (NTF) of the single-loop or cascaded SDM is $NTF = (1 - z^{-1})^L$. When the order L is high, the quantization noise is more effectively suppressed at low frequencies, and we have more gain at high frequencies. That implies that this function may not be suitable in lower OSR applications. The problem encountered in the noise shaping function is the large high frequency noise shaping gain for large L. The idling waveform at the comparator input becomes very large due to low comparator gain and makes the system to become unstable. We can modify the pure differentiating response by introducing poles into the NTF, and the NTF can be expressed as $NTF = \frac{(z-1)^n}{D(z)}$. The purpose of adding $D(z)$ is to flatten the frequency portion of the NTF as shown in Figure 1. According to Figure 1, we find that as the bandwidth is higher, the noise floor of $NTF = \frac{(z-1)^n}{D(z)}$ is effectively suppressed by $NTF = (1 - z^{-1})^L$. Since the NTF is simply an nth-order high pass function, we can design the bandwidth can be designed by determining the 3dB frequency of the filter, and the SNR can be determined by the filter order or the quantization bit numbers. In [2,8,12] a Butterworth or an inverse-Chebyshev high pass function is used for the design of the NTF denominator, and then proper zeroes can be added to its numerator to increase the in-band noise suppression.

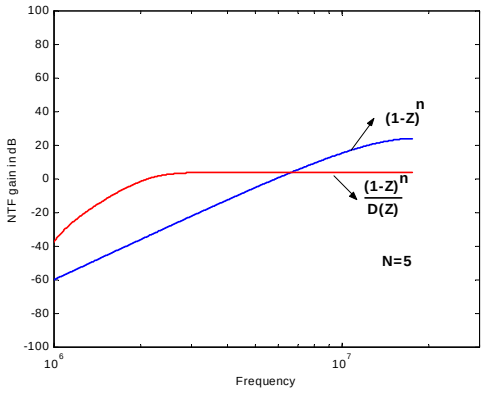


Figure 1. Modifying the NTF to reduce high frequency gain

In this paper, the NTF is designed by inverse-Chebyshev filter. Figure 2 shows the frequency response of an inverse-Chebyshev high-pass function. First, let us describe the

architecture and some disadvantage of the sigma-delta modulator with feedforward summation and local resonator feedbacks (FFSDM). The block diagram of FFSDM is shown in Figure 3.

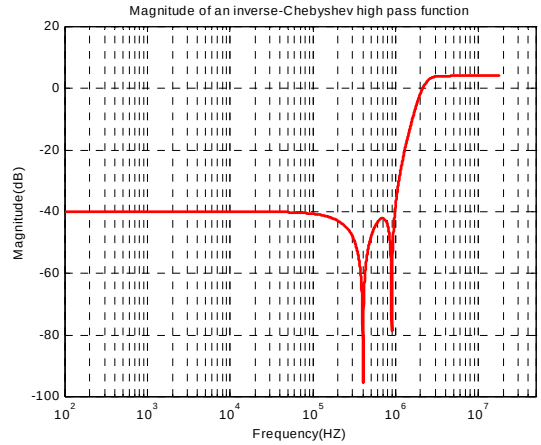


Figure 2. The frequency response of an inverse-Chebyshevhigh pass function

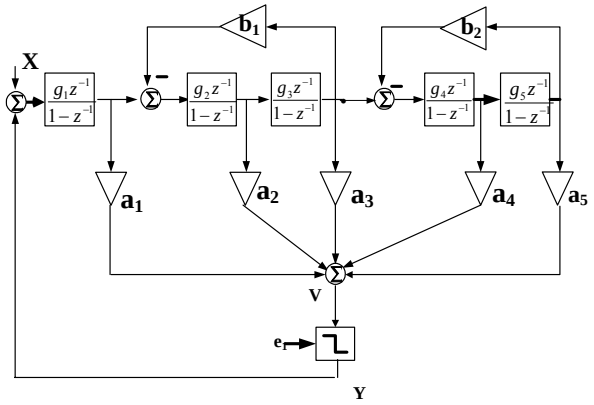


Figure 3. Linear model of a feedforward sigma-delta modulator

In FFSDM, it is possible to move the open-loop poles (which become the NTF zeros when the loop is closed) away from dc along the unit circle by adding a small negative-feedback term (r_i) around pairs of integrators in the loop filter. This causes the frequencies of infinite loop gain (and hence infinite noise attenuation) to be shifted away from dc to finite positive frequencies. The equation for a pair of integrators with feedback is

$$R(z) = \frac{z}{z^2 - (2-r)z + 1} \qquad (2)$$

The poles have a radius of 1 and a frequency ω,

$$\omega = a\cos(1 - \frac{r}{2}) \approx \sqrt{r} \quad \text{for} \quad r << 1 \qquad (3)$$

Equations (2) and (3) are derived by assuming that one of the integrators has a simple delay while the other does not. This can be accomplished in switched-capacitor circuits by correctly phasing the switches from the negative feedback network. A slightly less effective resonator can be built by using feedback around pairs of integrators, while allowing both integrators to have a z^{-1} delay term in the numerator. In this case, the poles move on a vertical line from the (1, j0) point away from the real axis and therefore do not exhibit infinite gain at the resonance frequency. The switched-capacitor implementation for the dual-delay integrator pair is simple and does not require double op-amp settling. To solve the coefficients, we can use Kuo's high-order SDM synthesis tool, HOST [7]. According to Mason gain theorem, the NTF of an even-order (N=2m) can be expressed as

$$\mathrm{NTF_{FF}} = \frac{N(z)}{D(z)}$$

where

$$N(Z) = \prod_{i=1}^{m}[(z-1)^2 + r_i] \qquad (4)$$

$$D(Z) = \prod_{i=1}^{m}[(z-1)^2 + r_i] + \sum_{i=1}^{m}([a_{2i-1}(z-1) + a_{2i}] \cdot \prod_{j=i+1}^{m}[(z-1)^2 + r_j]) \qquad (5)$$

By equating the $\mathrm{NTF_{FF}}(z)$ and the synthesized NTF(z), the SDM coefficient can easily be obtained.

The design flow is expressed as follows:
First, the coefficient r's are used to fit the zeros in the synthesized NTF(z). When r's are obtained, a's can also be obtained by equating their denominators. The coefficient g's are set to 1; this approach may limit the swing of the integrator but the coefficient can be adjusted to avoid overload. The stability of this architecture is decided by the noise power gain (NPG) that can be expressed as follows:

$$NPG = \frac{1}{\pi}\int_0^{\pi}(\left|NTF(e^{j\omega})\right|)^2 d\omega \qquad (6)$$

A large NPG may increase the high-frequency noise that may result in destabilization of the modulator [11], and cause the modulator to become unstable.

Although the FFSDM is a good architecture for wide bandwidth application, the multi-bit quantization may cause difficulties in the hardware implementation. By using the multi-bit quantizer in the FFSDM, a multi-bit DAC is required and the DAC may cause the performance degrading. Figure 4 shows the general model with DAC errors. The output of the SDM function with DAC errors can be derived as:

$$Y(z) = G(z)X(z) + H(z)E_Q(z) - G(z)E_D(z) \qquad (7)$$

where $G(z)=\frac{L(z)}{1+L\ (z)}$ is the signal transfer function (STF) and can be designed as a low pass filter; $H(z)=\frac{1}{1+L\ (z)}$ is the noise transfer function (NTF) and can be designed as a high pass filter.

According to equation (7), the DAC error cannot be shaped by *H(z)* and will appear in the base-band to increase total noise floor. Due to the nonlinear effects, the SNR will decrease significantly when the DAC error is large. Many architectures such as data weighted averaging algorithm (DWA) [9] and dynamic element matching (DEM) [3] can be used to solve this problem. Although DWA and DEM are invented to solve the nonlinearity problems of DAC in SDM, the solutions are still too complicated. A new SDM architecture without multi-bit DAC but has good performance is proposed in this paper, and the details are described in next section.

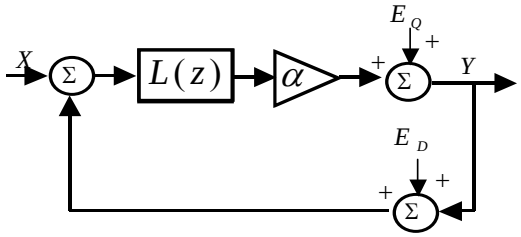


Figure 4. The linear block diagram of a general SDM with DAC error

3. A New Architecture of Wide Bandwidth Sigma-Delta Modulator

In the new SDM architecture, we use a 1.5-bit quantizer in the feedback path and thus eliminate the multi-bit DAC; we also use error cancellation scheme in the digital part to cancel the coarse quantization errors. We call this SDM as cascaded feedforward sigma-delta modulator (CFFSDM). The schematic diagram of this architecture is shown in Figure 5.

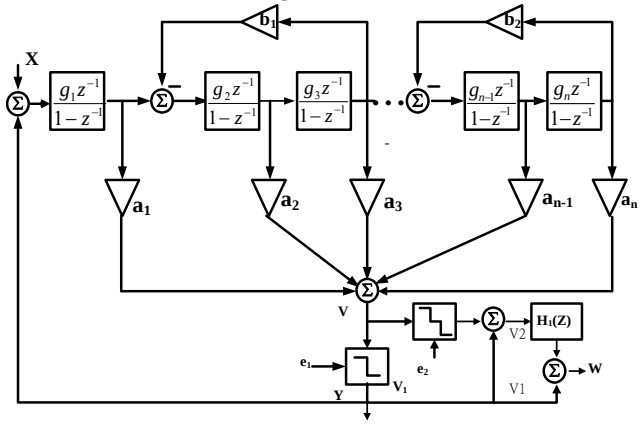


Figure 5. The architecture of cascaded feedforward sigma-delta modulator

For the topology shown in Figure 5, the loop filters are essentially identical:

$$L_0(z)=\frac{a_1}{z-1}+\frac{a_2}{(z-1)^2}+\frac{a_3}{(z-1)^3}+.....+\frac{a_n}{(z-1)^n} \quad (8)$$

Once the loop filter is set for optimum noise shaping, and thus the STF is fixed. Specifically,

$$G(z)=1-H(z)=\frac{L}{1+L} \quad (9)$$

where

$$H(z)=\frac{1}{1+L} \quad (10)$$

and

$$v_1=v+e_1\,. \quad (11)$$

The digital outputs v_1 and v_2 can be expressed as

$$v_1=Gu+He_1 \quad (12)$$

$$v_2=[(v_1-e_1)-v_1]+e_2 \quad (13)$$

If the digital filter H_1 is chosen to be

$$H_1=H=NTF\,, \quad (14)$$

then the output *w* becomes

$$w=v_1+H_1v_2=Gu+He_2 \quad (15)$$

In (15), the coarse quantization noise e_1 is cancelled in the ideal case. Therefore the output function of CFFSDM and the ideal output function of FFSDM with multi-bit DAC are identical. The CFFSDM does not only solve the nonlinearity of the multi-bit DAC problems but also has very good error resistance to the pole errors, gain errors, and coefficient variations. Although, we need a digital filter to maintain the same system performance with conventional FFSDM but as we know, the digital circuits are simpler and have lower area and noise than analog circuits. Therefore, our proposed architecture can reduce the analog circuit (no DAC requirement) and only need to add a digital filter. The simulation results are shown in Section V. The nonideality effects and error cancellation schemes are described in next section.

4. Nonlinearity Effects and Error Cancellation Schemes

The major analog imperfections of the CFFSDM are pole errors, gain errors, and coefficient variations, and they are described in the following subsections.

4.1 Pole Errors

The pole error is an important nonideality that can degrade the performance of the CFFSDM. This error is due to the finite integrator gain at dc (A_{dc}),

and can further shape the quantization noise. The transfer function of a delay and leaky integrator is:

$$H(z)=\frac{1}{z-(1-\frac{1}{A_{dc}})} \quad (16)$$

Therefore, the transfer function of *L(z)* in CFFSDM will become:

$$L(z)=\frac{a_1}{z-(1-\frac{1}{A_{dc}})}+\frac{a_2}{[z-(1-\frac{1}{A_{dc}})]^2}+\frac{a_3}{[z-(1-\frac{1}{A_{dc}})]^3}+.....+\frac{a_n}{[z-(1-\frac{1}{A_{dc}})]^n} \quad (17)$$

This effect may change the NTF and degrade the SNR.

4.2 Gain Errors

Mismatches between the sampling and integrating capacitors resulting in a gain error in the transfer function of a switched-capacitor integrator can be expressed as:

$$H(z)=\frac{1+\lambda}{z-1} \quad (18)$$

where $\lambda=\Delta C=(\Delta C_2/C_2)-(\Delta C_1/C_1)$ (19)

and ΔC is the relative capacitor errors of the integrators. Thereafter *L(z)* becomes:

$$L(z)=\frac{a_1(1+\lambda)}{z-1}+\frac{a_2(1+\lambda)}{(z-1)^2}+\frac{a_3(1+\lambda)}{(z-1)^3}+.....+\frac{a_n(1+\lambda)}{(z-1)^n} \quad (20)$$

This effect may change the pole location of the NTF, and may degrade the performance or make the modulator to become unstable.

4.3 Coefficient Variations

The coefficient variations may deviate *L(z)*, and thus change the desired NTF to an unknown status. The effect of coefficient variations may cause a coarse quantization noise e_1 through the leakage path. The output voltage in z-domain becomes:

$$V_{real}(z)=V_{ideal}+H_{leakage}(z)E_1(z) \quad (21)$$

Let us Assume small relative errors, and then the transfer function, $H_{leakage}(z)$, of the leakage noise can be approximated by a finite Taylor series expansion:

$$H_{leakage}(z)=\left.\frac{V_{real}(z)}{E_1(z)}\right|_{\substack{X(z)=0\\E_2(z)=0}}$$

$$=A_0+A_1\frac{(1-z^{-1})}{D(z)}+A_2\frac{(1-z^{-1})^2}{D(z)}+....+A_{M-1}\frac{(1-z^{-1})^{M-1}}{D(z)} \quad (22)$$

where coefficients $A_0, A_1, \ldots, A_{M-1}$ are functions of both the dc op-amp gain A_{dc} and the relative capacitor errors ΔC of the integrators. The filtering effects of factor $\frac{(1-z^{-1})^i}{D(z)}$ are dependent on the OSR.

In order to eliminate the leakage e_1 in the output, we use an adaptive filter with least mean square (LMS) algorithm and a dither injection scheme to correct the imperfection of the analog circuit [6,13]. The schematic diagram of the CFFSDM with error correction schemes is shown in Figure 6.

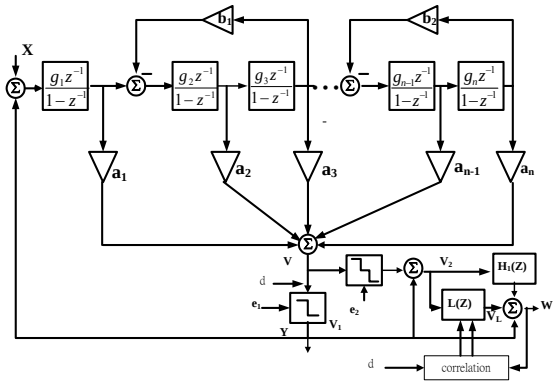


Figure 6. CFFSDM with error correction scheme

The main components of V_2 in Figure 6 are the negative 1.5-bit quantization noise ($-e_1$) and dither ($-d$); the z-transform is given by:

$$V_2=-E_1(z)-d(z)+E_2(z)\cong -E_1(z)-d(z) \quad (23)$$

And hence, the digital correction signal V_L in Figure. 6 is given by:

$$V_L(z)=V_2(z)L_c(z)\cong -(E_1+d)(w_0+w_1z^{-1}+w_2z^{-2}+\ldots+w_{m-1}z^{-(m-1)}) \quad (24)$$

where m coefficients w_i's form the vector $w=[w_0, w_1, \ldots w_{m-1}]^T$. Thus V_L is a negative estimation of the noise leakage. Since the exact values of the analog imperfection are a priori unknown, the parameters of the digital correction filter $L_C(z)$ must be adaptively controlled. The adding of a dither in front of the 1.5-bit quantizer behaves similarly to the quantization noise. Since the dither signal d_s follows the same parasitic leakage path toward the output as the quantization noise e_1, removing the dither signal from the output

requires the same operation as removing the quantization noise e_1 from the output. In other words, the minimization of the dither signal in the output is equivalent to the minimization of the noise leakage. Therefore adding a dither signal also can reduce the tone in the base band [8]. Although, we need a adaptive filter to maintain the system performance but as we know, the digital circuit have lower circuit noise and area than analog circuit. Therefore, it is worth to add a digital filter to maintain the whole system performance.

5. Simulation Results

Consider the circuit specifications of high-speed SDMs for xDSL system as expressed in Table 1:

Table 1. The desired circuit specifications of the SDM

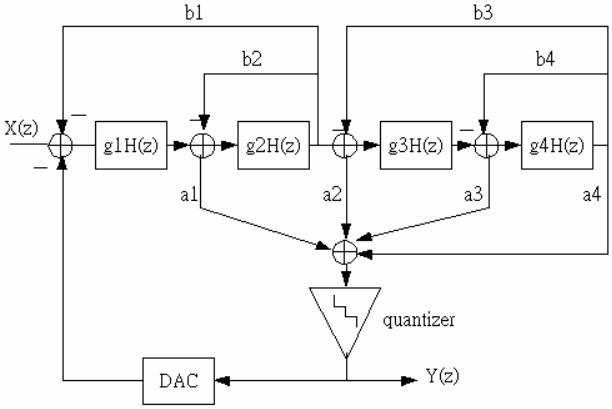
Specifications	Values
Peak SNDR	80dB
Dynamic Range (DR)	80dB
Modulator Order	≤ 4
Quantizer Bit	≤ 5
Oversampling Ratio	≤ 20
Signal Bandwidth	2.5MHz
Maximum Stable Input	-6dB

Using the automatic high-order SDM synthesis tool (HOST) [7] that proposed by Kuo et al. to design this SDM can obtain the specifications shown in Table 2.

Table 2. Specifications of the synthesized FFSDM

Specifications	Values
Peak SNDR	86dB
Dynamic Range (DR)	88dB
Modulator Order	4
Quantizer Bit	4
Oversampling Ratio	12
Signal Bandwidth	2.5MHz
Sampling Frequency	60MHz
Maximum Stable Input	-6dB
Modulator structure	FFSDM

The structure and the corresponding modulator coefficients are shown in Figure 7 and the output spectra are shown in Figure 8.



Coefficient	Value	Coefficient	Value	Coefficient	Value
g1	3.72725	a1	0.663192	b1	0.0132411
g2	1.18157	a2	0.582002	b2	0.0493528
g3	1.10037	a3	0.30669	b3	0.0776458
g4	0.136377	a4	0.463003	b4	0.0667221

Figure 7. The structure and its coefficients of a fourth-order four-bit FFSDM where

$$H(z)=\frac{z^{-1}}{1-z^{-1}}$$

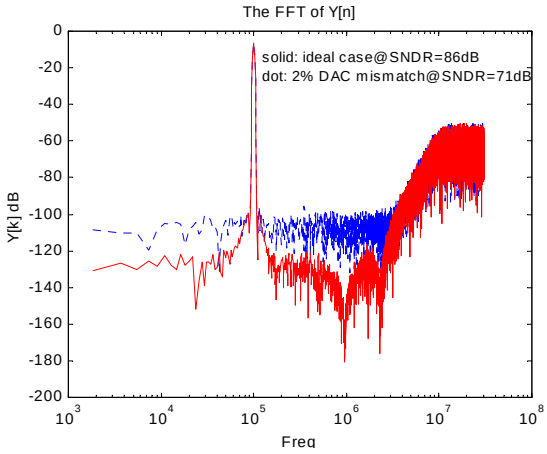


Figure 8. The output spectra of FFSDM with ideal case and DAC mismatch

According to Figure 8, we find that the DAC mismatch is the most serious problem in FFSDM. Therefore, the data-weighted averaging (DWA) [8] can be used to reduce the DAC mismatch. However, DWA may increase the analog circuit complexity.

By using the CFFSDM architecture, the DAC mismatch problem can be eliminated and only need to design a digital cancellation. The same circuit specifications of FFSDM can be applied to CFFSDM and the specifications of the synthesized CFFSDM can be obtained and are shown in Table 3,

and its coefficients are shown in Table 4.

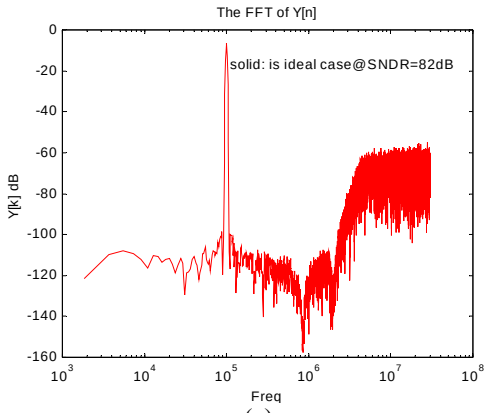
Table 3. Specifications of the synthesized CFFSDM

Specifications	Values
Peak SNDR	82dB
Dynamic Range (DR)	84dB
Modulator Order	4
Quantizer Bit	1.5 bit for feedback path 5 bit for output path
Oversampling Ratio	12
Signal Bandwidth	2.5MHz
Sampling Frequency	60MHz
Maximum Stable Input	-6dB
Modulator structure	CFFSDM

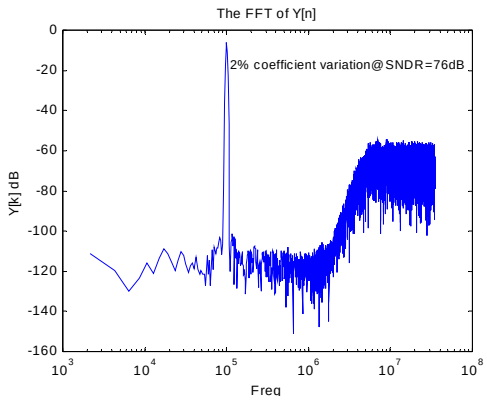
Table 4. Coefficients of the four-order five-bit CFFSDM

Coefficient	Value	Coefficient	Value	Coefficient	Value
g1	0.9	a1	0.9	b1	0.08
g2	0.6	a2	0.6	b2	0.08
g3	0.5	a3	0.5	b3	0.08
g4	0.2	a4	0.2	b4	0.05

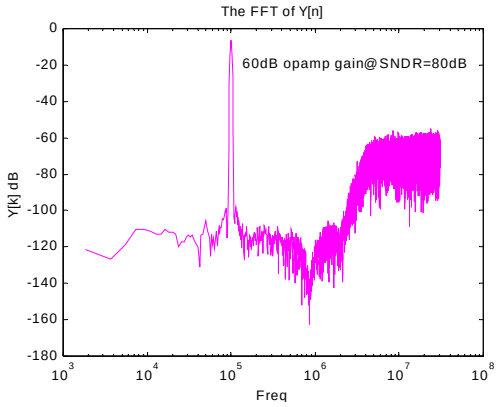
The output spectra are shown in Figure 9 with coefficient variations and finite opamp gain. According to Figure 9, the CFFSDM can reduce the analog circuit complexity effectively and the coefficient variations can be reduced by careful layout techniques.



(a)



(b)



(c)

Figure 9. The output spectra of CFFSDM (a) ideal case, (b) with coefficient variations, and (c) with finite opamp gain

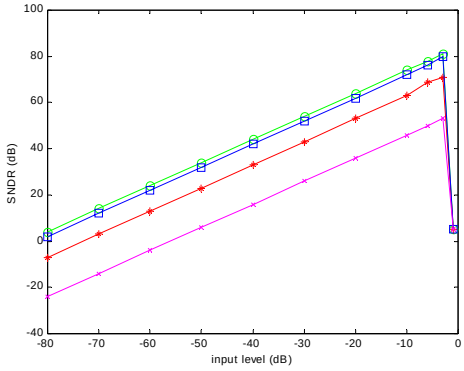


Figure 10. The SNDR plot of the CFFSDM (○: for ideal case, *: with 5% coefficient variations, □: $A_{dc} = 60dB$, x: 1.5-bit quantizer output)

As using the CFFSDM architecture with 1.5-bit quantizer in the feedback loop, the output spectra are shown in Figure 9, and Figure 10 is the SNDR of CFFSDM with various conditions. From Figure 10 we find that the DAC error is eliminated, but the gain error becomes more serious due to the 1.5-bit quantization noise leakage of the output. By employing the adaptive filter and dither signal the simulation result is shown in Figure 11. The result exhibits that the SNDR increases by several adaptive cycle times, and finally the adaptive error-correction process converges to an optimum value. From Figure 11, we find the SNDR of the CFFSDM with error correction scheme is almost the same as that of the ideal case, and Figure 12 is the time-domain outputs of all integrators in CFFSDM. The comparisons of the various different architectures are showed in Table 5.

Table 5. The comparisons of the various different architectures

Architectures / Specifications	MASH 2-2	FFSDM	CFFSDM
Order	4	4	4
Quantizer bit	4	4	1. 5@5
OSR	16	12	12
Sampling ratio (MHz)	60	60	60
SNDR with ideal case (dB)	88	86	82
SNDR with A_{dc}=60dB (dB)	77	84	80
SNDR with 2% DAC mismatch (dB)	82	71	82
SNDR with 2% coefficient variation (dB)	78	84	76

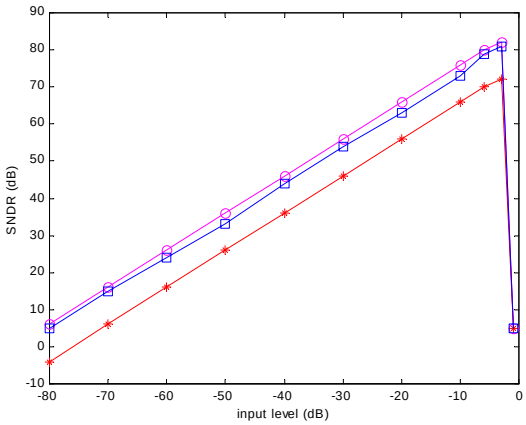
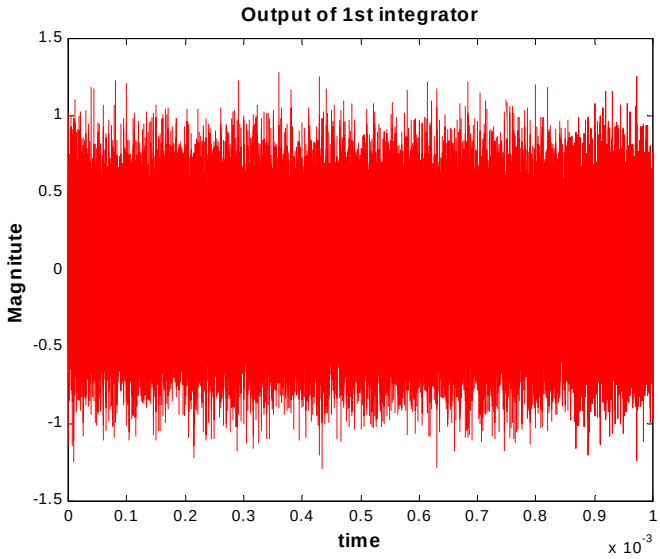
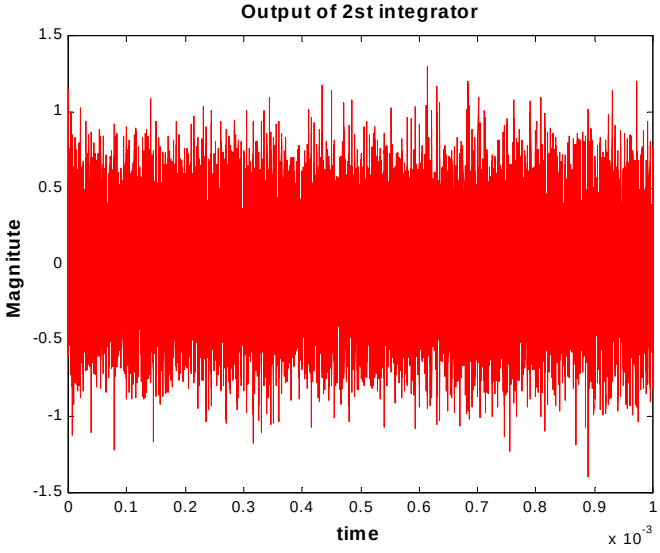


Figure 11. The SNDR plot of the CFFSDM (○: for ideal case, *: with 5% coefficient variations and $A_{dc} = 60dB$, □: adaptive filter output)





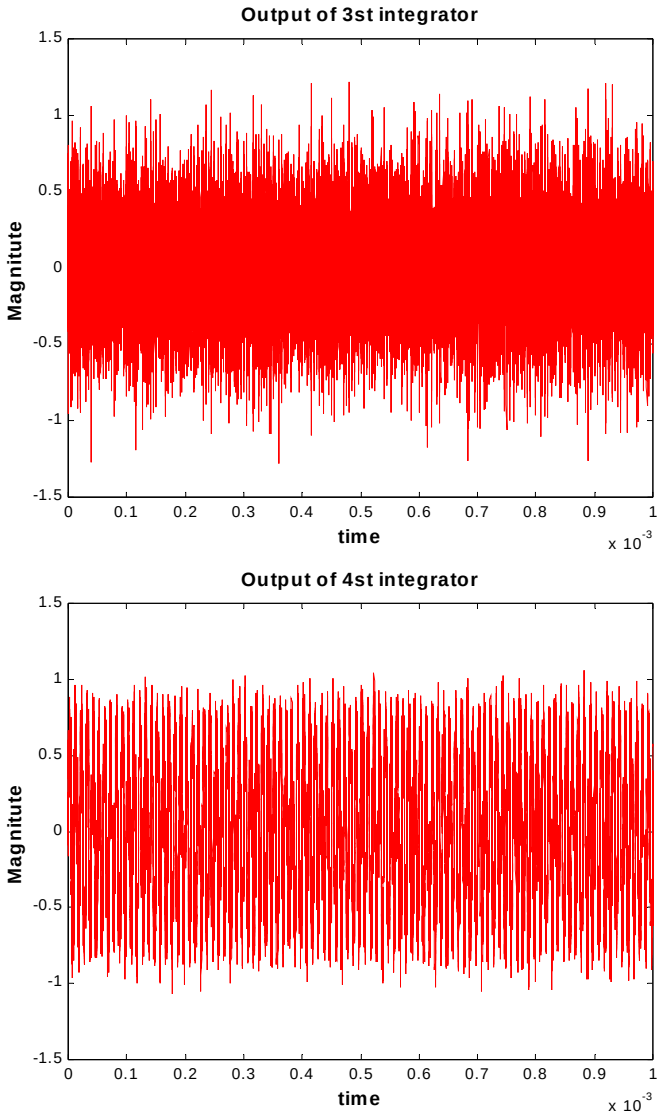


Figure 12. Time-domain outputs of all integrators in CFFSDM

6. Conclusion

In the conventional wide bandwidth SDM design, people use multi-bit quantizer with multi-bit DAC to implement the SDM. The nonlinearity of the multi-bit DAC causes the difficulty and complexity of the design and implementation of the wide bandwidth SDM. In the proposed CFFSDM, we use 1.5-bit quantizer to overcome the problems caused by the multi-bit DAC. The coarse quantization error caused by the 1.5-bit quantizer can be cancelled by the adaptive filter with least mean square algorithm and a dither injection scheme in the digital part. The simulation shows this new architecture is almost as good as the ideal case. The proposed architecture provides an alternative choice of easier implementation of the wide bandwidth sigma-delta modulator.

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