Dynamic Bias Circuits for Efficiency Improvement of RF Power Amplifier

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Abstract

This work presents a dynamic gate bias circuit for bias control to maximize power added efficiency based on the class-A two-stage power amplifier. The proposed circuits are composed of two NMOS transistors, a capacitor for coupling RF input signal, and four resistors for bias. The circuit is implemented by means of the bias control at the two-stage power amplifier to improve the overall power added efficiency and delivers 22dBm output power at 2.4 GHz. The circuit can improve power efficiency and linearity for small RF signals. The simulation indicates that the efficiency is improved more than 100%, and at 0 dBm the input signal has 5–15dB of IMD_3 improvement compared with that without dynamic bias circuit. The output power of 22dBm at the output stage can be applied to the transceivers of IEEE 802.11b and Bluetooth applications [8].

***Key Words*:** CMOS, Dynamic Bias Circuits, Linearity, Power Added Efficiency, Power Amplifier, RF.

1. Introduction

Because most of the power is consumed at the amplifier stage in a RF circuit, the efficiency of a power amplifier is one of the most important concerns in portable radio units. Many efforts of high efficiency RF power amplifier have been proposed, such as DC–DC converter [1], digital control using switch control, and bias switch [2]. However, the solutions proposed by [1] and [2] are not satisfied for portable wireless application due to high complexity and high cost circuits. Switching mode power amplifiers, such as Class-D, Class-E, and Class-F amplifiers, have high power efficiency, but they work as non-linear operations and may generate interferences for the adjacent channels. The linearities of class-A and class-AB amplifiers are good for power amplifier applications, but the power efficiency of these two types are poor [3]. Power consumption depends on the DC bias voltage, and higher DC bias voltage consumes more power [3]. The RF input signal fluctuates, and the small signal needs small DC bias voltage. If the bias point can dynamically vary in a class-A amplifier according to the varying envelope of the incoming RF input signal, power can be saved significantly [4].

For the varying bias point consideration in class-A amplifiers, Yang et al. proposed ideas to reduce supply voltage or current (dual bias controlling) [5]. Shin et al. proposed an adaptive bias circuit to reduce the DC quiescent current to have higher power efficiency for the one-stage power amplifier [3, 6, 7]. This paper proposes another approach for varying bias to reduce the DC power at a small RF signal input to have the two-stage power amplifier to work more efficiently. The simulation indicates that the power amplifier with our dynamic bias circuit can improve the power efficiency more than 100% at 0dBm input and linearity compared with the

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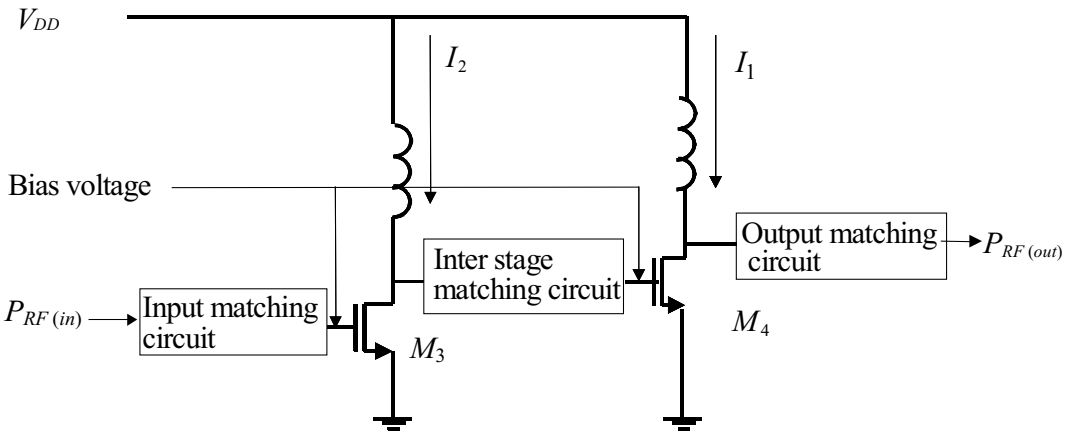

Figure 1. Block diagram of a two-stage amplifier.

power amplifier without the dynamic bias circuit.

2. Operation Principles of the Dynamic Bias Circuit

The definition of power added efficiency (PAE) for a two-stage amplifier is illustrated in Figure 1 and Eq (1).

$$\text{PAE} = \frac{P_{RF(out)} - P_{RF(in)}}{P_{DC}} = \frac{P_{RF(out)} - P_{RF(in)}}{(I_1 + I_2) \cdot V_{DD}} \qquad (1)$$

PAE is the ratio of the delivered power at the desired *RF* frequency to the product of the total current $(I_1 + I_2)$ and the voltage of the DC power supply (V_{DD}). If P_{DC} is constant, the power efficiency of a small *RF* signal is reduced. The dynamic bias circuit may change the bias point following $P_{RF(in)}$ to bias gate voltages of M_3 and M_4. Figure 2 shows the proposed dynamic bias circuit. C_1 and M_1 are the coupling capacitor and detector respectively for the input signal. The sizes of C_1 and M_1 should be as small as possible to minimize the effects on the input matching circuit. R_1 and R_2 are bias resistors

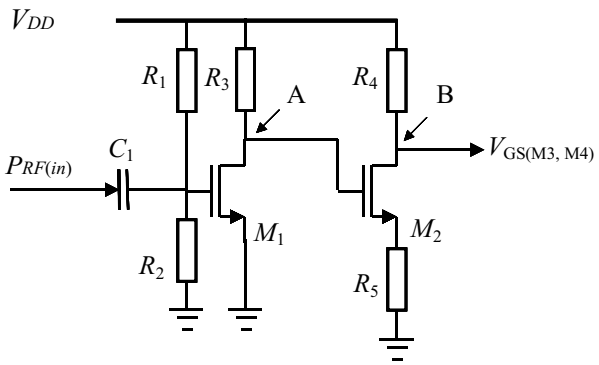

Figure 2. The proposed dynamic bias circuit.

of M_1, and the bias voltage is designed to close to its threshold voltage.

When $P_{RF(in)}$ increases, it leads an increased harmonic in the drain current of M_1, and it results the voltage to decrease on node A and at the meantime the voltage on node B raises the bias voltage of M_3 and M_4. Figure 3 demonstrates the input power versus node A and node B. The dis-

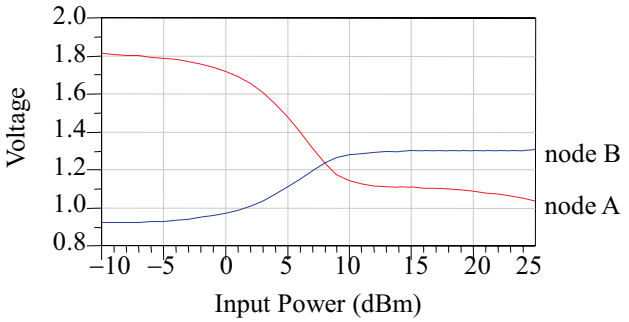

Figure 3. The input power versus node A and node B.

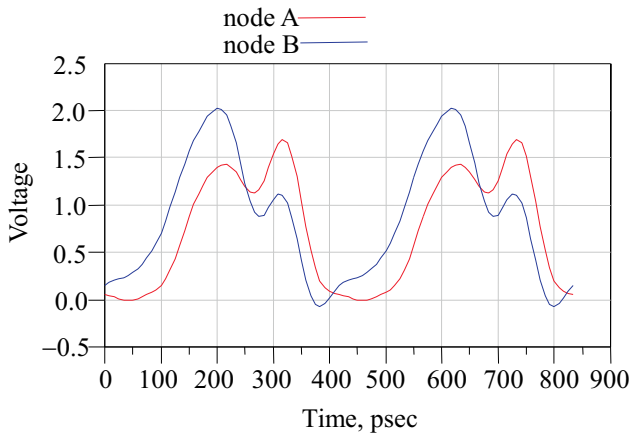

Figure 4. Harmonic on node A and B when $P_{RF(in)}$ is in higher power input.

tortions of the AC harmonic on node A and node B are shown in Figure 4, in case $P_{RF(in)}$ is in the higher power input. In order to restrict the harmonic effect on node B we need a LPF (low pass filter) circuit at the output. In Figure 5 node B is connected to the gate of M_4 and the inter stage circuit to generate a DC voltage to bias M_3 and M_4.

The large value of $Cgs_{(M4)}$ is able to perform good performance for the LPF function, without any of the

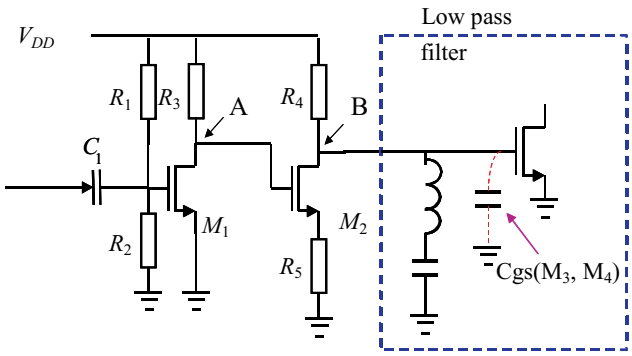

Figure 5. Low pass filter on output stage and driver stage.

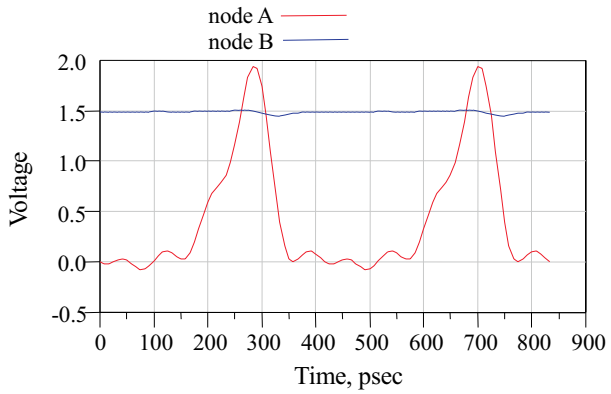

Figure 6. The harmonic of node A and node B when node B connects between M_4 and the inter stage circuit.

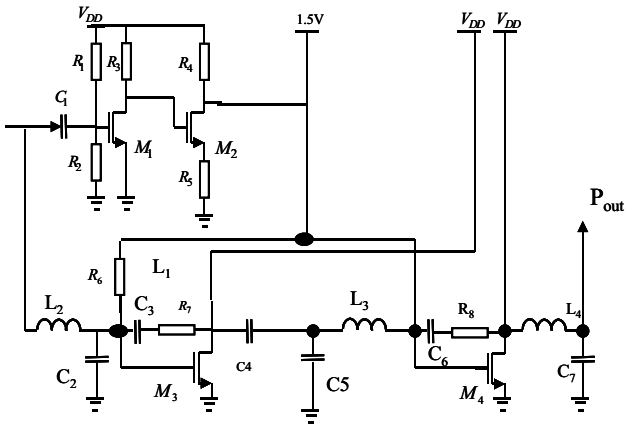

Figure 7. The schematic diagram of a two-stage amplifier with a dynamic bias circuit.

harmonic distortion on the output waveform, as shown in Figure 6, when $P_{RF(in)}$ connects a RF signal. The schematic diagram of a two-stage amplifier with a dynamic bias circuit is shown in Figure 7.

The minimum voltage $V_{GS(M3,M4)}$ is determined by $V_{DS(M2)}+V_{R5}$. When $P_{RF(in)}$ is in a high power situation, there is no load current going through M_2 and thus the major concern of this circuit is to decide the optimum control range of $V_{GS(M3,M4)}$ on node B. For a class-A power amplifier, it always consumes DC power even though there is no RF input signal. The dynamic bias circuit can adjust the bias point according to the amplitude of the RF input signal and therefore can save DC power significantly.

3. Design of the Dynamic Bias Circuit

For a given input power, the voltage of node B is an important issue because it can decide the optimized gate voltages of M_3 and M_4. If the voltage is too low, the transistor may enter the linear region and the power efficiency will be scattered. Therefore, the optimized bias can be formulized as functions of the output power. Equation (2) and the I_D-V_{DS} curve (Figure 8) describe the relationship of the operating point and RF signal swing range when the amplifier operates as a class-A amplifier.

$$Z_{opt} = \frac{Voltage\ Swing}{Current\ Swing}$$

$$V_{knee} = (V_{GS} - V_{threshold})$$

$$P_O = \frac{(V_{breakdown} - V_{knee})^2}{2z_{opt}} = \frac{(Voltage\ Swing)^2}{2Z_{opt}}$$

$$\Rightarrow I_D = \sqrt{\frac{2 \cdot P_O}{Z_{opt}}} \tag{2}$$

According to equation (2), the output power P_O can be expressed as a function of the DC drain current I_D, and Z_{opt} is an optimum load impedance when the transistor is in the saturation region. The large signal transconductance G_m can be calculated as follows:

$$G_m = I_D \div (V_{GS} - V_{threshold}). \tag{3}$$

Substitute equation (3) into (2) and we can find V_{GS} as follows:

$$V_{GS} = \frac{1}{G_m} \cdot \sqrt{\frac{2 \cdot P_O}{Z_{opt}}} + V_{threshold}\,. \tag{4}$$

If the transistor is in the saturation region, G_m is a con-

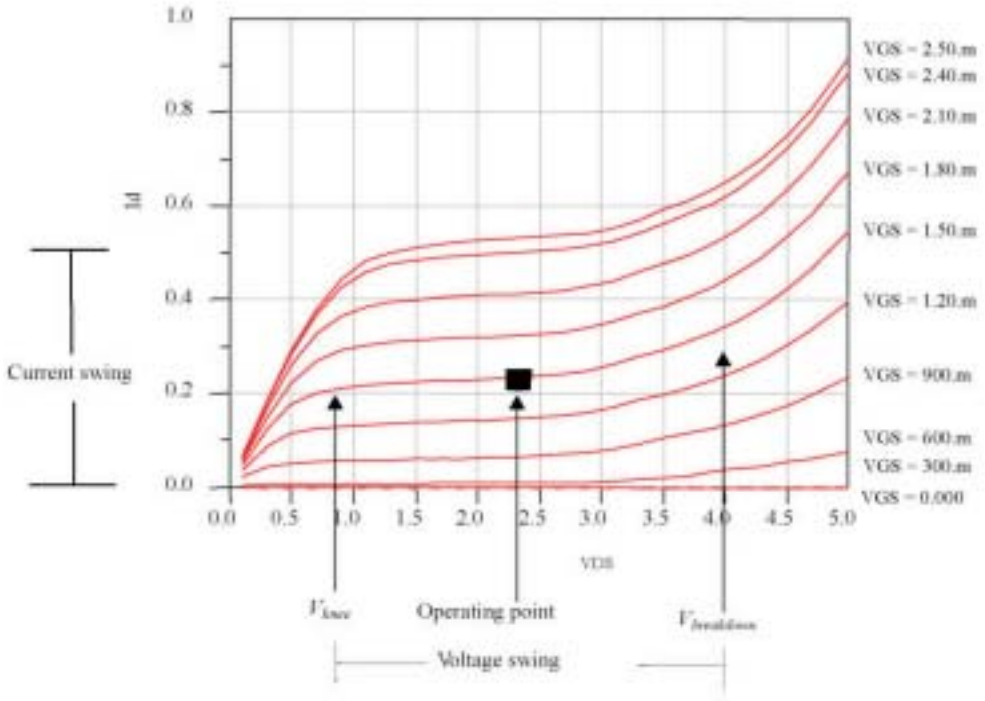

Figure 8. I_D-V_{DS} curve and the operating point in a class-A amplifier.

stant value. Therefore, the minimum $V_{GS(M3,M4)}$ is equal to $V_{GS} - V_{threshold}$, and the control range is from the operating point (1.5V) to the minimum voltage $V_{GS(M3,M4)}$. The value of $V_{GS(M3,M4)}$ is approximately equal to 0.9 V.

4. Design of a Two–stage Amplifier

In order to achieve a high power gain, a two-stage common source amplifier circuit topology is proposed in this paper and is shown in Figure 9. The first stage is designed for the power gain, and the second stage is designed to match for maximum power output. Both transistors, M_3 with 320 μm gate width and M_4 with gate width of 960 μm, are biased in class-A mode, and the operating voltage is set to 1.5 V by external DC power supply in order to achieve higher linearity at the output.

The primary design strategy of this work is to work with each stage separately. The secondary design strategy is to match the second stage output matching circuit towards the first stage input matching circuit. The stabilities of the individual stages and the combination of the first and second stages are checked. The load pull simulation is used to

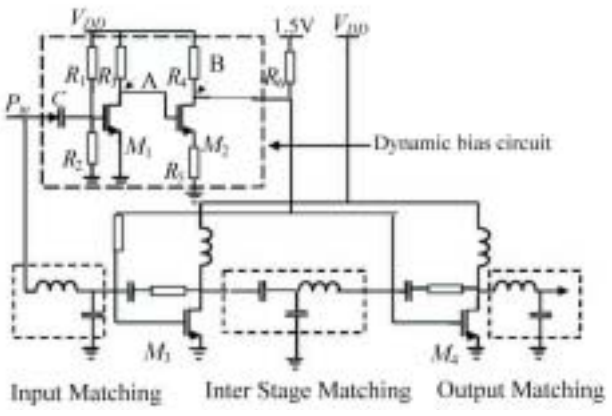

Figure 9. The schematic diagram of the proposed two-stage power amplifier with a dynamic bias circuit.

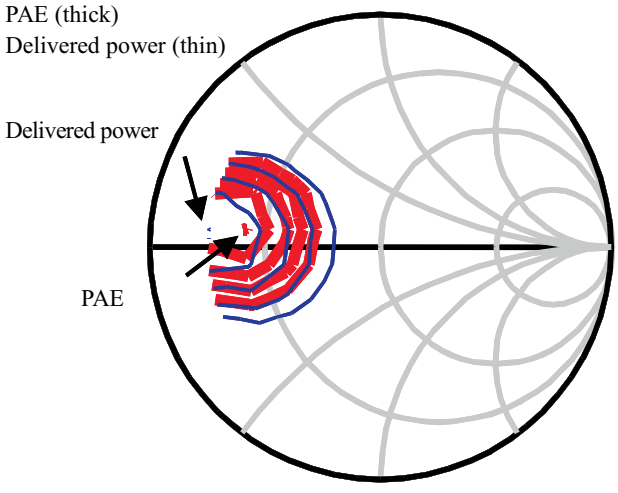

Figure 10. Simulation of PAE and the delivered power.

realize the maximum output power to find the optimum output impedance, Z_{opt}. The contour of the *PAE* and the delivered power simulation is shown in Figure 10.

5. Comparisons and Analyses

According to equation (4), $V_{GS(M3,M4)}$ can be determined as a function of the output power, P_O, and the large transconductance, G_m. If the power gain is constant, $V_{GS(M3,M4)}$ is also a function of the input power. The comparison charts of the power amplifier with the dynamic bias circuit and that without the dynamic bias circuit are shown in Figures 11 and 12 respectively. The simulation results are summarized in Table 2 and Table 3.

Table 1. Summarization of PAE, gain, and output power

	PAE	GAIN	P_{output}
at −1dB	25%	17 dB	22 dBm

Table 2. Summarization of PAE versus output power

P_{output} (dBm)	6 dBm	12 dBm	18 dBm	21 dBm
w. circuit	1.6%	6%	20%	26%
w/o. circuit	0.4%	2.1%	7.13%	23%

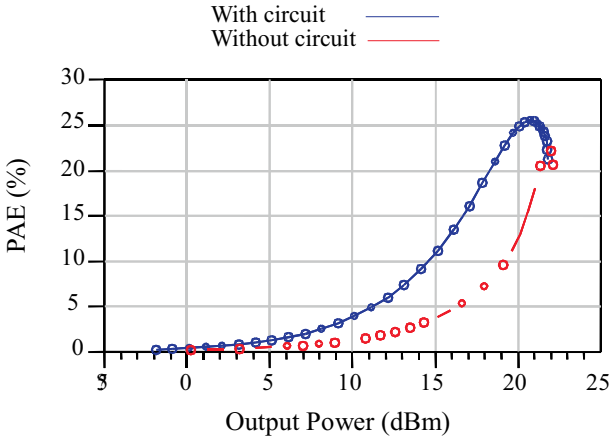

Figure 11. PAE versus output power.

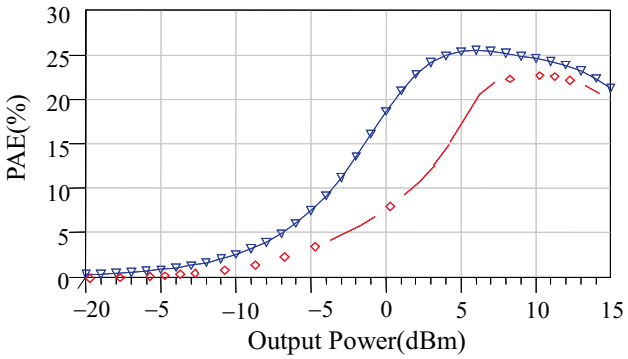

Figure 12. PAE versus input power.

6. Linearity Consideration

The simulation of the bias voltage on node B versus two-tone IM_3 (third-order inter modulation) is depicted in Figure 13. The result exhibits lower bias on node B causes less IMD_3 harmonic.

The two-tone IM_3 and pi/4 DQPSK modulation ACPR (adjacent channel power ratio) are made to evaluate the linearity of the amplifier. The simulation shows that the two-stage amplifier with dynamic bias circuit has 5–15dBc IM_3 decreasing in a wide range of output power compared with the original amplifier without dynamic bias circuit. The IM_3 versus output power is shown in Figures 13 and 14 shows the transmitted spectrum.

This work is designed and simulated by the parameters of the TSMC 0.25 um RF model and the VLSI layout

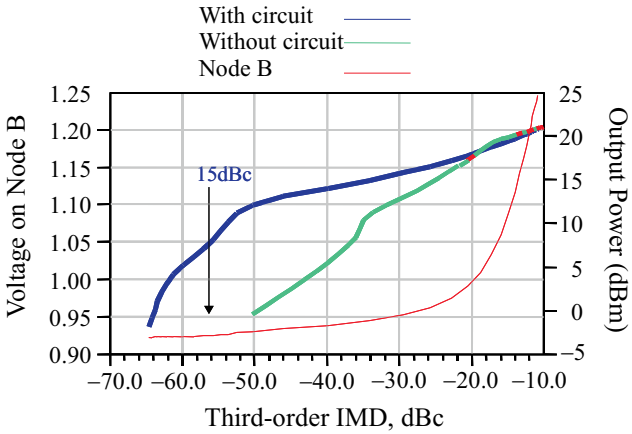

Figure13. IMD_3 versus Vbias on node B and output power.

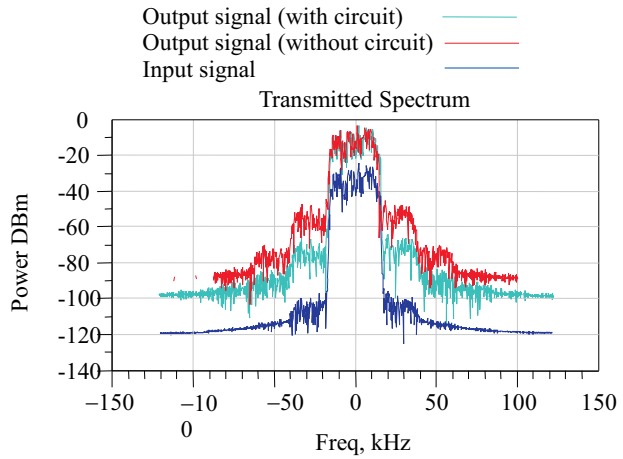

Figure 14. IMD_3 versus output power.

Table 4. Summarization of the key parts of the layout size of the chip

	M1 / M2	M3 / M4	C2 / C5/ C7	L2 / L3 / L4	R1 / R2 / R7 / R4
Gate Width(um)	80 / 80	320 / 960	30 / 24 / 60		162/ 54 / 21.6/ 27
Nr				2.5/ 2.5/ 3.5	

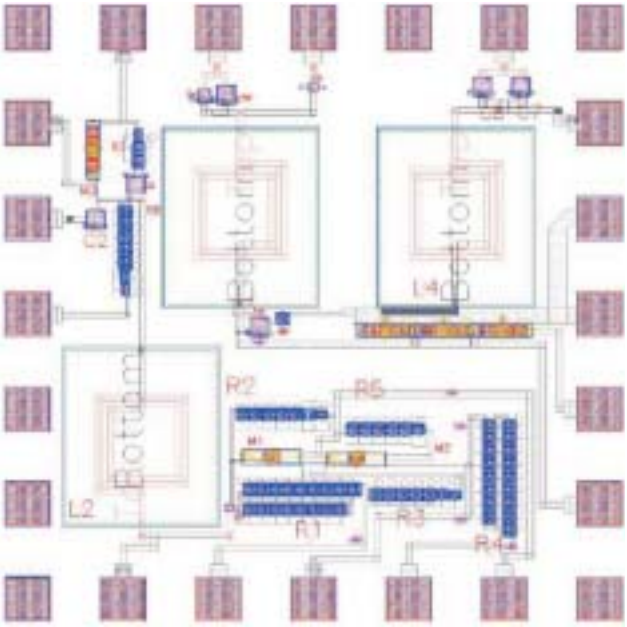

Figure 15. VLSI layout diagram of the amplifier with dynamic bias circuits.

diagram is shown in Figure 15. The smallest size of the model for M_1 and M_2 is 80um as the gate width. However, the proposed circuit needs gate width of M_1 and M_2 as small as possible. If the gate width of M_1 and M_2 can be reduced further, the performance can be even better. The summarization of the key parts of the layout size of the chip is listed in Table 4.

8. Conclusion

In this paper a dynamic bias circuit for class-A power amplifier is proposed. This dynamic bias circuit is applied to a two-stage common source amplifier. The proposed bias circuit can improve the power efficiency and linearity of low RF input signal significantly. The simulation indicates that the efficiency is improved more than 100% at 0 dBm input signal and at least 15 dBc IM_3 improvement and about 10 dBc lower sideband decreasing on ACPR. The overall power added efficiency and linearity are improved and it can deliver 22 dBm output power at 2.4 GHz.

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Manuscript Received: Mar. 22, 2004
Accepted: May 21, 2004