Application of Novel Digital Techniques for the Design of High Sensitivity Limiting Amplifier

Yang-Han Lee and Kuo-Ting Lin

Department of Electrical Engineering
Tamkang University
Tamsui, Taipei Hsien, Taiwan, R. O. C.

Abstract

In this letter we utilize the novel digital techniques (TW, DRMC, DS) to improve the sensitivity of the limiting amplifier. The Time Window (TW) technique can ignore the positive & negative trigger noises within the window close time. The Delay Racing Memory Counter (DRMC) technique can eliminate the positive trigger noises within the window open time. The Delay Sum (DS) technique can solve the negative trigger noise around the signal transition from low to high. The experimental results are also presented.

Key Words: Limiting Amplifier, Digital Techniques

1. Introduction

This paper proposes novel digital techniques (the Time Window (TW), the Delay Racing Memory Counter (DRMC) and the Delay Sum (DS) techniques) to process the positive and negative trigger noises while the received signal being weak at the input of the conventional limiting amplifier [1], [2] to improve the receiving sensitivity as shown in Fig.1. The TW technique can ignore the positive & negative trigger noises (i.e., (a) and (b) in Fig.1) within the window close time (t_{window}) by the time window counter. The DRMC technique can eliminate the positive trigger noises (i.e., (c) in Fig.1) within the window open time (t_{open}) by the delay racing memory counter. The DS technique can filter out the negative trigger noises around the signal transition from low to high (i.e., (d) in Fig.1) by the delay sum circuit.

System Description : The system block diagram for the high sensitivity limiting amplifier is shown in Fig.2. The input signal from the output of conventional limiting amplifier is put to the DS circuits with the delay value of τ_{sum}. Then the signal is processed by the DRMC (delay value of τ_{delay}, logic circuit and the memory counter with the size of N_{bit} bits) and TW (the time window counter with the size of N_B bits, the threshold value of time window, N_{TH}, and master-slave T-FF) circuits as shown in Fig.2. Finally, we can get the output signal by half the frequency of input signal without suffering from those trigger noises generated at the received weak signal.

2. Circuit Design

The high sensitivity limiting amplifier circuit is implemented by the ALTERA chip (EPM7128ELC84-15) in terms of VHDL as shown in Fig.3. We use the dual window counters (TWINDOW0 and TWINDOW1 with the threshold of N_{TH}) to control the TW circuits. The simulated trigger noises are added to the input signal by the SNXOR. Then the noisy signal (XOROUT) is put to the DS circuits to filter out the negative trigger noises around the signal transition from low to high. The OROUT is input to DRMC circuits with two memory counters (SCOUNT0 and S_DCOUNT1 for the signal without and with delay, respectively). The SUBTRACT (= SCOUNT0-S_DCOUNT1) and MONITOR (when the input is equal to or not equal to 111111, this circuit will decide the received signal is data or noise, respectively) will eliminate

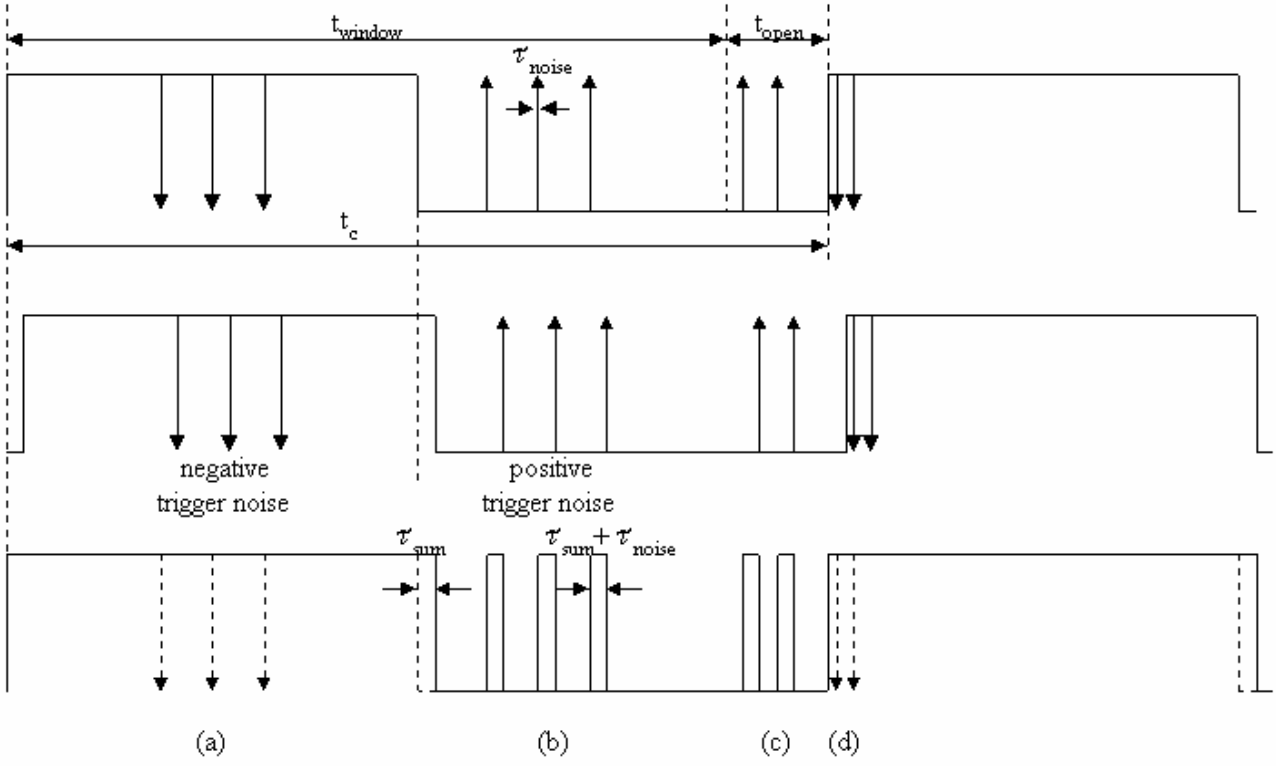

Figure 1. The Signal and Trigger Noises at the Output of Limiting Amplifier. t_{window} is the Window Close Time. t_{open} is the Window Open Time

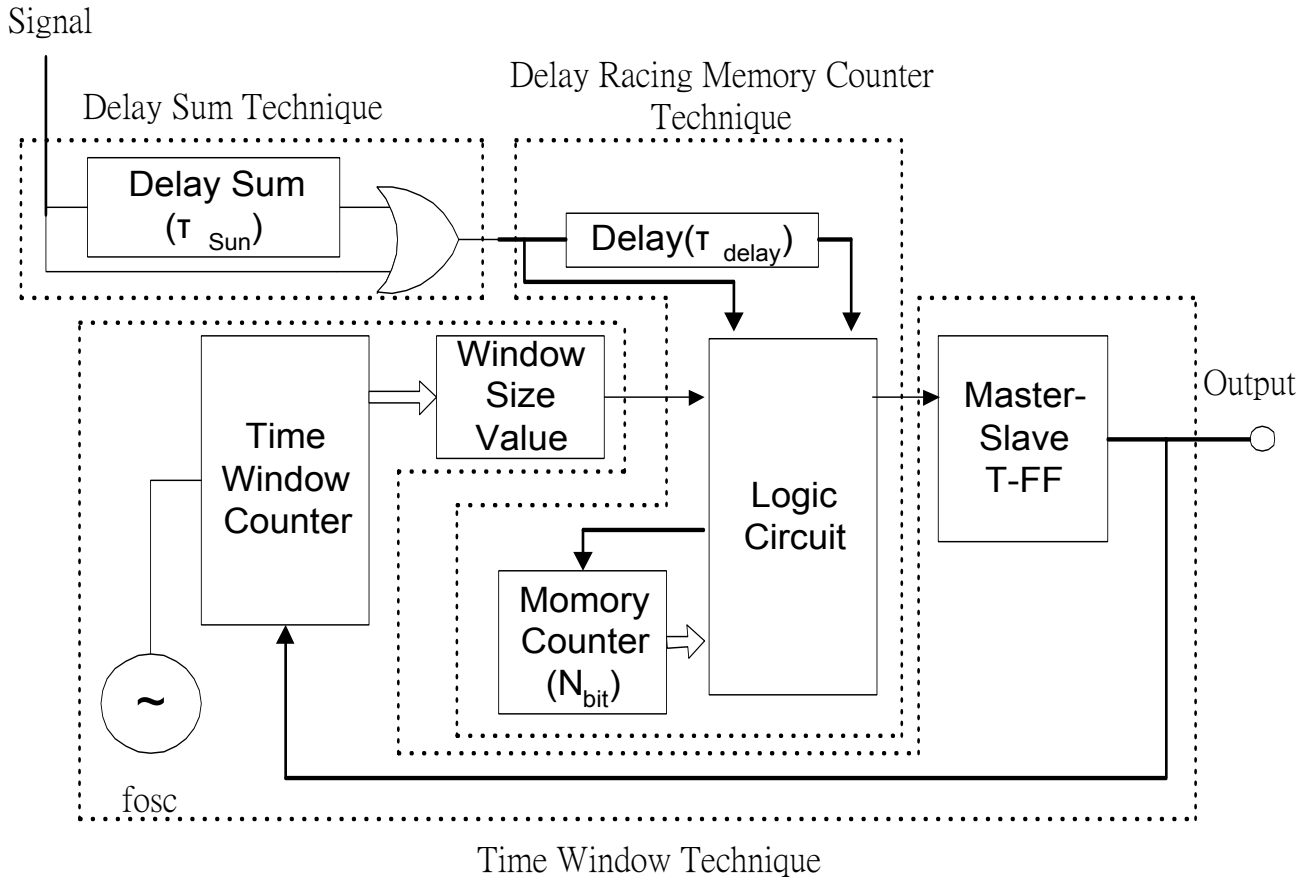

Figure 2. The Block Diagram for the Time Window, the Delay Racing Memory Counter, and the Delay Sum Techniques.

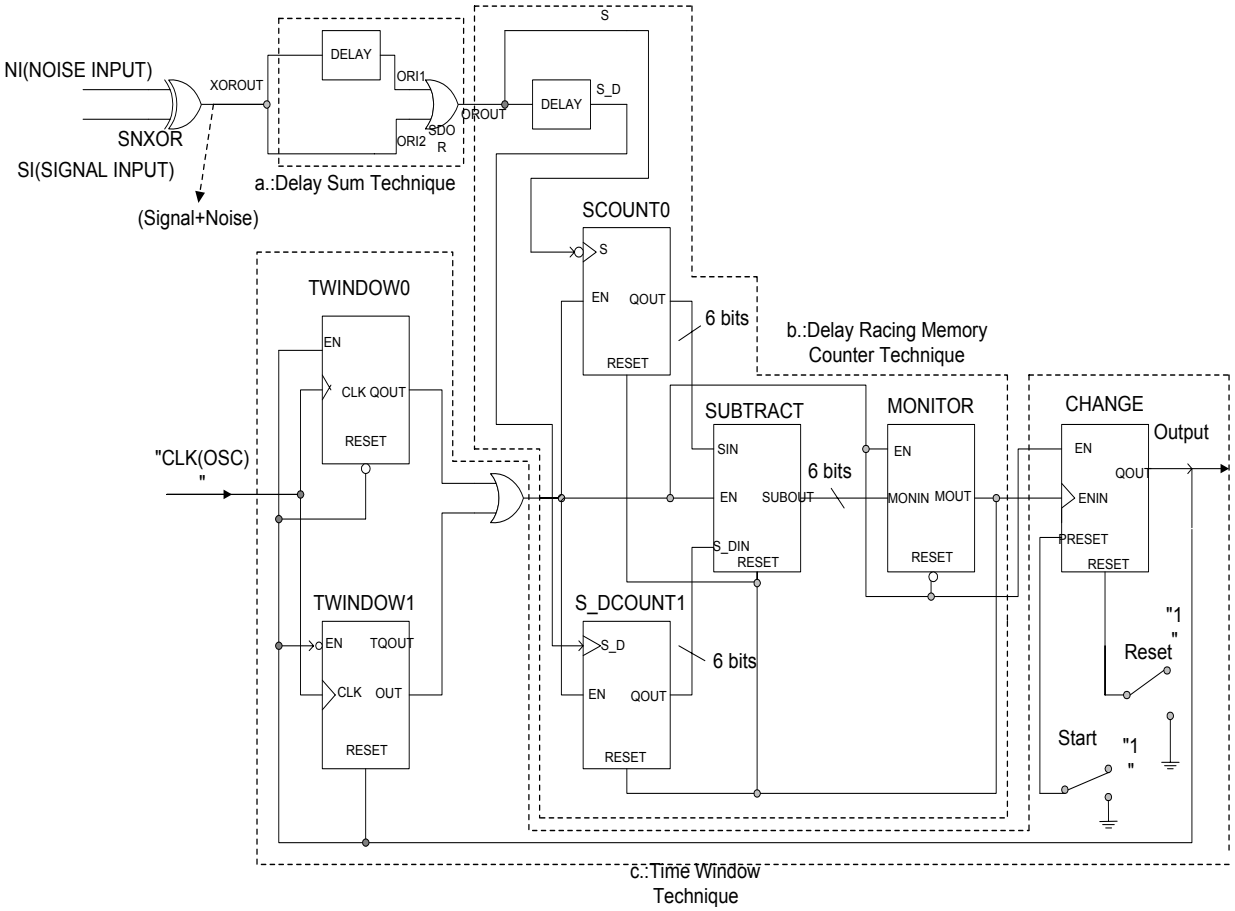

Figure 3. The High Sensitivity Limiting Amplifier Circuit

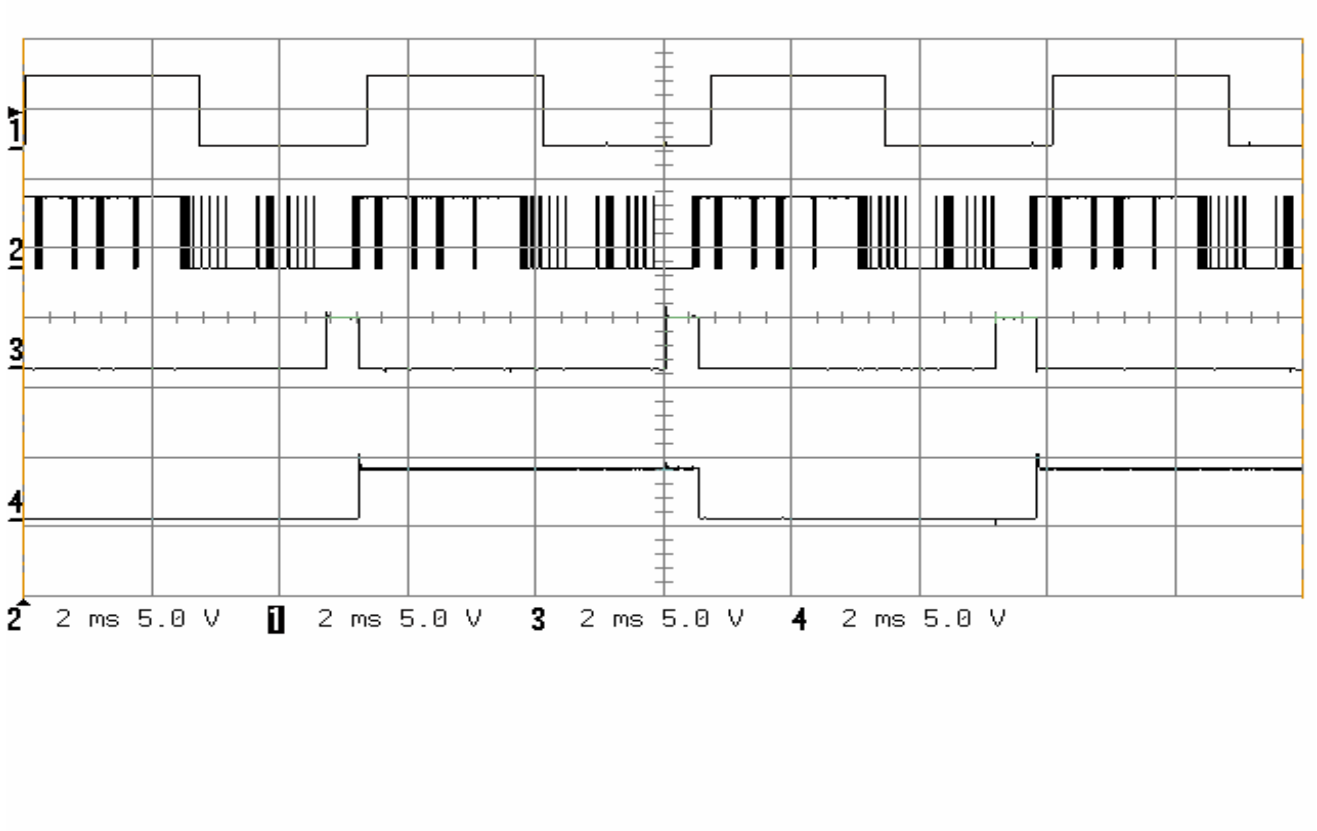

Figure 4. Experimental Results for the High Sensitivity Limiting Amplifier.

the positive trigger noises within the window open time. The decision signal (i.e., 111111 is detected) from the MONITOR will force the CHANGE to alternate its output and this will generate the output signal without trigger noises by the half frequency of the input signal.

3. Experimental and Simulation Results

The experimental results for the input signal of 183.48Hz and the clock of 8KHz (CLK) with the τ_{sum} = 230us, τ_{delay}= 10us and τ_{noise} < 1us are shown in Fig.4. The sizes of the memory counter and the time window counter are chosen to be 6bits (N_B= N_{bit}=6). The threshold value of time window, N_{TH} is set to be 37 (100100). The 1 and 2 in Fig.4 represent the signal without and with the trigger noises, respectively. The 3 in Fig.4 represents the total window time for the TW to be 5.45ms with the window close time in terms of "0" (t_{window}=4.75ms, 87.16% of the total window time) and the window open time in terms of "1" (t_{open}=0.7ms, 12.84% of the total window time). The 4 in Fig.4 represents the output signal frequency of the high sensitivity limiting amplifier to be 91.74Hz without the trigger noises

4. Conclusion

The high sensitivity limiting amplifier with the novel digital techniques (TW, DRMC, DS) are proposed in this letter. Those techniques can eliminate the positive & negative trigger noises within the conventional limiting amplifier. The TW , DRMC and DS can deal with the positive & negative trigger noises within the window close time, the positive trigger noises within the window open time, and the negative trigger noise around the signal transition from low to high, respectively. Then we can get the output signal at this high sensitivity limiting amplifier without being contaminated by the trigger noises. These techniques are implemented by the ALTERA chip and experimental results are given for the input signal frequency of 183.48Hz and the clock of 8KHz (CLK) with τ_{sum} = 230 us, τ_{delay}= 10us and τ_{noise} < 1us to obtain the output noise free signal of this novel high sensitivity limiting amplifier with the frequency of 91.74Hz.

Acknowledgements

This work was supported by the National Science Council (NSC 87-2622-E002-016).

Reference

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Manuscript Received: Apr. 12, 1999
Revision Received: Apr. 26, 1999
And Accepted: May. 31, 1999