Feedback-Controlled Enhance-Pull-Down BiCMOS for Sub-3-V Digital Circuit

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***abstract*-This paper describes a new feedback-controlled chanced-pull-down BiCMOS (FC-EPD-BiCMOS) logic scheme for the low-supply-voltage operation. Through the use of the feedback-controlled enhanced-pull-down structure, the driving capability is improved and biploar transistor saturation during operation period is avoided. Based upon the proposed structure, both static and differential logic gates are developed. The new BiCMOS three-input NAND gate offers 35% reduction in the propagation delay time as compared to conventional BiCMOS circuits at 2.5 V supply voltage. The proposed three-input FC-EPD-BiCMOS CPL XOR/XNOR gate has 33% improvement in delay time as compared to conventional BiCMOS 3-input XOR/XNOR gates at 2.4 V supply voltage.**

I. Introduction

BiCMOS technology is being actively employed in a wide spectrum of ULSI's for its high-speed, low power, and high density characteristics. In using the conventional BiCMOS logic for low-supply-voltage applications, however, the gate delay increases significantly when the power supply voltage is decreased. This is because the effective voltage applied to the MOS device is lowered by the inherent built-in voltage (V_{be} ~ 0.7V) of the bipolar devices in the conventional BiCMOS totem-pole type circuit. To solve this problem, new logic circuits, such as the BiNMOS [1] and C-BiCMOS [1]-[2], have been proposed and studied. But BiNMOS has a small performance leverage over the CMOS and the advantages of the C-BiCMOS are considerably offset by the additional process complexity and cost in the fabrication of the p-n-p bipolar transistor.

The reason for the degraded performance of the conventional BiCMOS circuits at the power supply voltage below 4 V [3],[5] is briefly reviewed as follows. As shown in Fig.1(a), when the input makes a low to high transition, the maximum gate voltage applied to the nMOS MN1 is

$$V_{gs} = V_{dd} - 2V_{be} \quad (1)$$

where V_{gs} is the gate-source voltage, V_{dd} is the supply voltage, and V_{be} is the base-emitter voltage when the bipolar transistor is turned on. As the supply voltage is reduced, V_{be} is nealy fixed and thus Vgs is reduced accodingly, resulting in severe drain-current degradation.

The main concept behind QC-BiCMOS is the avoidance of this Darlington circuit to eliminate the voltage loss due to V_{be}. The schematic inverter configuration of the QC-BiCMOS [5] is shown in Fig.1(b). The base of the n-p-n biploar transistor Q2 is driven by the pMOS MP2. In this pull-down operation, the drain-source voltage of MP2 is reduced by the V_{be} of Q2. However, the gate-source voltage is not affected. Since the drain current depends slightly on the drain-to-source voltage in the saturation region, the delay time is less influenced by the voltage drop V_{be}.

The reason for the degraded performance of the QC-BiCMOS circuit at low voltage and at low loading is brifely discribed below. When the input makes a low-to-high transition, the base of the n-p-n bipolar transistor Q2 for pull-down operation is driven by the pMOS MP2. During this pull-down operation, the drain-source voltage of MP2 is reduced by the V_{be} of Q2, This makes MP2 operated in the linear region and the drain current of MP2 (the base current of Q2) decreases simultaneously. Especially when the circuit is operated at low supply voltage, the drain current of MP2 is further degraded severely. Low base current also makes Q2 operated in the low gain region and decreases the collector current. Thus the speed is degraded.

Due to the same reason, the previously proposed BiCMOS logic circuits ,for low-voltage or low-loading operation, such as complementary BiCMOS, BiNMOS, merged BiCMOS [4], and quasi-complementary BiCMOS(QC-BiCMOS) [5] do not have high-speed

advantage at low supply voltage or low loading operation conditions.

Although the transiently-saturated full-swing BiCMOS (TS-FS-BiCMOS) logic [6] for low-supply-voltage applications has been proposed as shown in Fig.1(c). But the TS-FS-BiCMOS needs the additional process complexity and cost for the p-n-p bipolar transistor fabrication. Moreover, when the input logic structure is complex, the parasitic capacitances of logic unit contributed to the base node of the bipolar transistor Q2 increase the turn-on time of Q2 which results in speed performance degradation of the TS-FS-BiCMOS.

The purpose of this paper is to propose and analyze a novel full-swing feedback-controlled enhanced-pull-down BiCMOS (FC-EPD-BiCMOS) structure with definite speed leaverage over the conventional BiCMOS circuits even at the supply voltage below 2.5-V. The FC-EPD-BiCMOS logic has two units: the internal circuit used to realize the logic functions whereas the external circuit used to realize the driving unit. The output capacitance load is completely separted from the logic block. Due to new circuit technique, a complex logic can be implemented in a single gate and obtain a short delay.

II. Feedback-Controlled Enhanced-Pull-Down BiCMOS Logic(FC-EPD-BiCMOS)

The proposed new circuit structure called the feedback-controlled enhanced-pull-down BiCMOS (FC-EPD-BiCMOS) is shown in Fig.2(a). When the input signal makes a low-to-high transition, Q1 is turned off and MP2 remains in the on state for a while due to the feedback CMOS inverter FBI1. The base current of Q2 is supplied by MP3 and MP2 from V_{dd}. Thus, there is no drain-source and source-gate voltage loss during the pull-down operation, which achieves high speed performance under low power supply condition. Q2 continues to drive the load until the output voltage nearly reaches zero. Thus, Q2 achieves full-swing operation. Although Q2 saturates, this does not slow the next pull-up transition because the excess minority carriers of Q2 are discharged immediately after the pull-down transition through MN3 which is turned on when the output signal is low and the feedback signal from the inverter FBI1 is pulled high.

When the input signal makes a high-to-low transition, MP1 is turned on and Q1 drives the load until the output voltage nearly reach V_{dd}-V_{be}. It is worthy to note that during the pull-up transient just after Q1 is cut off (when the output rises to a value of about V_{dd}-V_{be}), the feedback CMOS inverter FBI2 brings the output to the magnitude of the supply voltage through the help of the inverter FBI1.

Because the base current of Q2 is provided by V_{dd}, the base current of Q2 in this structure is larger than that in the other conventional BiCMOS circuits and the good speed performance can be achieved under low loading conditions. This solves the problems in the conventional BiCMOS, which has poor speed performance as compared with CMOS under low loading conditions.

For the low voltage operation, the feedback controlled enhanced-pull-down circuit technique is employed to enhance the circuit speed up to a level which has sufficient performance leverage over the conventional BiCMOS circuits. This circuit is controlled by the feedback CMOS inverter FBI1. When the output voltage is low enough to turn on the pMOS of the feedback CMOS inverter FBI1, its output voltage is high and MP2 is turned off. It can eliminate the dc current from power supply through MP3 and MN3. Thus the static power dissipation after the pull-down transition can be decreased. At the same time, MN3 is turned on and the base of Q2 is discharged. This makes Q2 turned off before Q1 is turned on, which decrease switching current and power dissipation. Similarly, when the input signal is low, MP3 is turned off and Q1 is turned on. The feedback signal is initially high and MP2 stays in the off state. When the output voltage level is high enough to turn on the nMOS of FBI1, the MP2 changes to the on state for the next operation period.

The feedback CMOS inverter FBI1 must be design carefully, taking both the base charge retention and the relief from the shallow saturation into account. Because of this feedback-controlled discharging circuit, the outflow of the base charges can be minimized in the pull-down transition. This technique can also avoid the large short-circuit current during the next transition. It can also achieve good speed performance at low supply voltage operation.

The proposed general structure of the FC-EPD-BiCMOS logic gates are shown in Fig.2. This structure can be separated into two units as shown in Fig.3(b). It can be seen that the CMOS logic circuit is seperated from the output node. Thus the parastic capacitance load of the CMOS logic to the output node can be avoided and good speed performance can be obtained, especially when a complex function is implemented in the same gate. The delay times of the FC-EPD-BiCMOS three-input NAND gate shown in Fig.2(c) versus supply voltage are shown in Fig.3 where the data of conventional BiCMOS gates are also presented. It can be seen that the supply voltage dependence of delay times in the FC-EPD-BiCMOS gates is the smallest. This is because the drain current of MP3 (base current of Q2) is provided by V_{dd} in the pull-down operation. Therefore, the output level can reach the ground level more easily than those in other BiCMOS gates. The speed performance under different load capacitances in the new BiCMOS logic is also superior to that in other conventional circuits as shown in Fig.4.

III. Differential Feedback-Controlled Enhanced-Pull-Down BiCMOS Logic

Several differential logic families have been proposed for circuit speed improvement. Among the differential logic families [7], the complementary pass-transistor logic (CPL) shown in Fig.5 is the most attractive one because of high-speed and low-power-dissipation characteristics [8]-[9]. Besides, the CPL has good performance in speed and power dissipation at low power supply voltage [8]. The CPL consists of complementary inputs/outputs, nMOS pass-transistor logic network with zero threshold voltage, and output static inverter. The pass transistors function as pull-up and pull-down devices. The pMOS latch can be designed with minimum device dimensions so that the pull-up function can be completed in the given cycle time. The output static inverters offer high driving capability and improve the speed performance. In order to solve the problems of the BiCMOS logic circuits under low-supply-voltage operation, new BiCMOS differential logic is developed by combining both CPL and the FC-EPD-BiCMOS..

An 3-input XOR/XNOR gate is shown in Fig.6. Fig.7 shows the delay characteristics of the XOR/XNOR gate with different output buffers (CMOS,QC-BiCMOS and FC-EPD-BiCMOS). It can be seen that the CPL XOR/XNOR with new FC-EPD-BiCMOS buffer of Fig.2(a) has a smallest delay as compared with the same CPL gates with CMOS or QC-BiCMOS buffer. Moreover, the speed performance of the new BiCMOS buffer is better than that of the CMOS buffer even under the small output loading. The same superiority is also observed in the simulated delay characteristics versus supply voltage as shown in Fig.8.

IV. Conclusion

In this paper, new feedback-controlled enhanced-pull-down BiCMOS logic is proposed and analyzed. Two key circuit design techniques are adopted to enhance the speed performance under low voltage operation. One is the separation of logic unit and buffer unit, which enable the complex logic function implementation in a single gate with short delay. The other is the the carefully designed feedback-controlled enhanced-pull-down structure. Which makes the FC-EPD-BiCMOS logic has the better speed performance than other conventional BiCMOS circuits. This technique also achieves high-speed full-swing operation under sub-3-V operation. Both load dependence and supply voltage dependence of gate delay times are also released with this technique. HSPICE simulated results have successfully verified the function and performance of the proposed BiCMOS gates and the combined CPL BiCMOS logic gates. It is believed that the FC-EPD-BiCMOS is quite promising for BiCMOS ULSI applications in sub-3-V regime.

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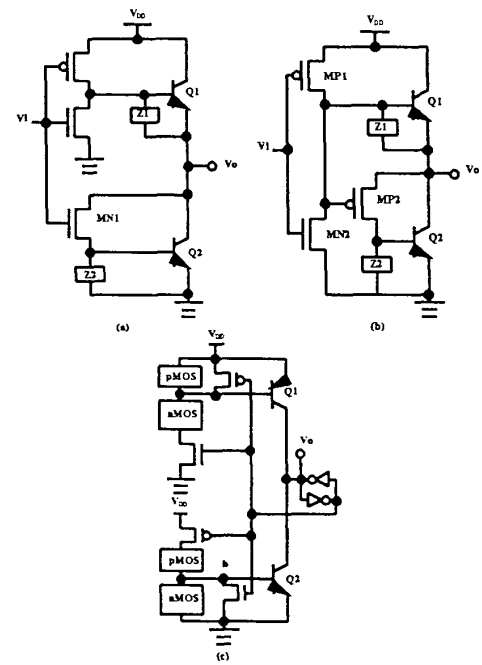

Fig. 1. Schematic circuits of (a) conventional (Darlington-type) BiCMOS inverter (b) QC-BiCMOS inverter (c) TS-FS-BiCMOS

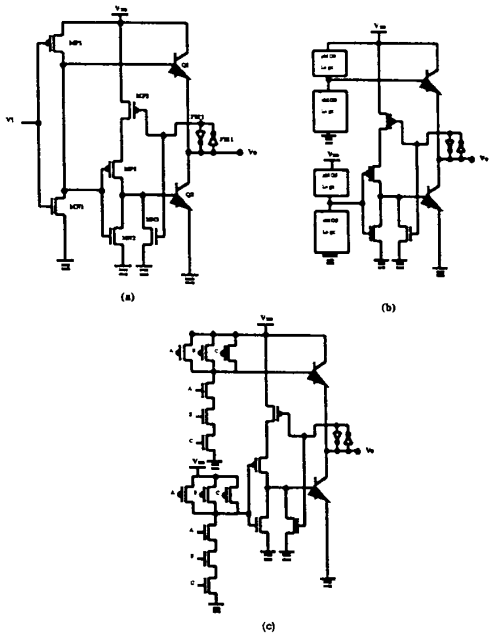

Fig. 2. Feedback-controlled enhance-pull-down BiCMOS(FC-EPD-BiCMOS (a) inverter; (b) general structure; (c) 3-input NAND gate.

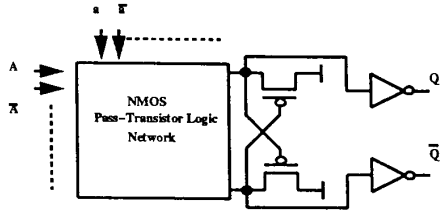

Fig. 5. Basic CPL circuit schemetic structure

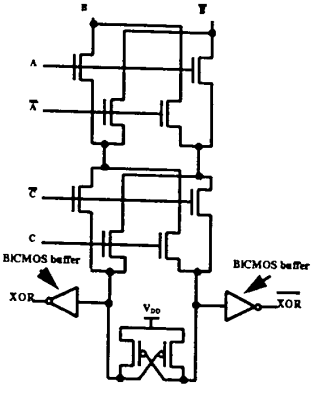

Fig. 6. CPL BiCMOS 3-input XOR/XNOR gate .

3-input NAND Gate with 0.2 pF Capacitance

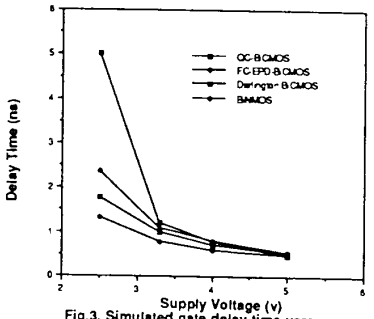

Fig.3. Simulated gate delay time versus supply voltage.

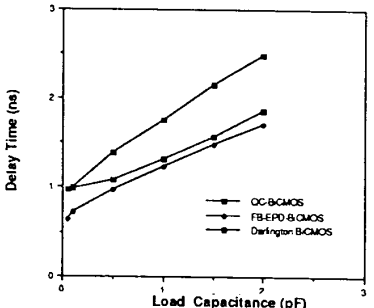

Fig.4. Simulated gate delay time versus load capacitance.

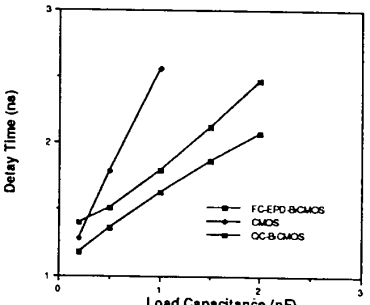

Fig.7. Simulated gate delay time versus load capacitance for the circuit of Fig.6.

3-input XOR/XNOR Gate with 0.2pF Capacitance

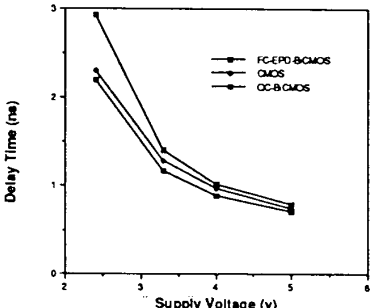

Fig.8. Simulated gate delay time versus supply voltage for the circuit of Fig.6.