Low-Voltage Low-Power CMOS True-Single-Phase Clocking Scheme with Locally Asynchronous Logic Circuits

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Abstract--New CMOS differential logic circuits, called asynchronous latched CMOS differential logic (ALCDL) circuits, are proposed and analyzed. The ALCDL can implement a complex function in a single gate and achieve high operation speed without dc power dissipation. New CMOS differential latches, which can be used to prevent extra transitions and reduce the power dissipation, are also proposed. A new clocking scheme is designed by locally using the ALCDL circuits and the entire system is synchronized to a single global clock. As compared to the conventional true-single-phase clock system, the loading of the global clock line and transient noise induced by precharge operation can be largely reduced. Simulation results show that the new clocking scheme and logic circuits benefit in high-speed and low-power performances, especially in low supply voltage.

I. INTRODUCTION

Conventional true-single-phase clocking scheme has been shown to benefit in high-speed and low-power performances [1],[2]. However, dynamic logic circuits induce large transient current spikes in the simultaneous precharge operation. Moreover, the conventional latches cause extra transitions which increase the power dissipation.

Asynchronous circuits avoid clock-related timing problems by enforcing a simple communication protocol between parts of the circuits [3]-[5]. However, the drawback to self-timed circuits are the hardware and signaling overhead involved in the local communication and in any timing constrains that are required by particular choices of signaling protocols. The enable/disable CMOS differential logic (ECDL) circuit has been shown to have good speed performance for complex gates [4]. However, the ECDL is operated without generating the completion signals and has difficulty in synchronizing and communicating between systems. Therefore, asynchronous designs are more difficult to implement than their synchronous counterparts.

In this paper, new CMOS true-single-phase clocking scheme is proposed. The logic circuits in the pipelined systems are implemented by new asynchronous logic circuits, called precharged asynchronous latched CMOS differential logic (H-ALCDL) and predischarged asynchronous latched CMOS differential logic (L-ALCDL). They are shown to have higher speed and lower power dissipation than ECDL. New differential latches are also proposed to synchronize the signals between adjacent pipelined systems and prevent the extra transitions of the conventional clocked CMOS latches. The new true-single-phase clocking scheme is designed by locally using the ALCDL circuits and synchronized by the new differential latches.

II. CIRCUIT TECHNIQUES AND CLOCKING SCHEME

Fig. 1(a) and 1(b) show the general circuit structure and clock timing of the conventional true-single-phase clocking scheme, respectively [1],[2]. When the clock falls (rises), the N-section (P-section) is in the precharge phase. The nodes N_1, N_2, ..., Nn (P_1, P_2, ..., Pn) are simultaneously precharged to V_{DD} (GND). The previous evaluation result is held at node Ln (Lp). A large transient current spike is induced in the power supply which may cause power supply variations.

Fig. 2(a) shows the block diagram of the asynchronous systems implemented by ECDL circuits [4]. The global clock line is not required and each block is controlled by the enable signal Ei generated from the previous block. Fig. 2(b) shows the ECDL circuit structure. When Ei-1 makes a low-to-high transition, Si is low and the sense amplifier (P1, P2, N1, and N2) is disabled. The output signals Qi and $\overline{Qi}$ are precharged to V_{DD}. When E_{i-1} makes a high-to-low transition, Si is high and the sense amplifier is enabled. Depending on the input signals, a pair of complementary signals is formed

at the output nodes Qi and $\overline{Qi}$. The enable signal Ei for the next block is also generated after the operation of the sense amplifier. Fig. 2(c) shows the timing diagram of the input/output and the enable signals of the ECDL circuit.

Fig. 3(a) shows the block diagram of the new true-single-phase clocking scheme. The internal logic circuits of the N-section (P-section) is implemented by asynchronous circuits H-ALCDL (L-ALCDL). Each pipelined section is synchronized by cascading new differential latch N-latch (P-latch). The global clock line is only used to control the first gate of the asynchronous circuits and the latches. Thus the total clock load can be reduced and the design of the clock buffer can be eased. Moreover, the locally asynchronous circuits are not simultaneously precharged. Therefore the large current spike induced in the precharge operation of the conventional true-single-phase systems does not exist in the new system.

Fig. 3(b) and 3(c) show the H-ALCDL and L-ALCDL circuits, respectively. The H-ALCDL (L-ALCDL) circuit has two operation phases, namely, the precharge phase and the evaluation phase. In the precharge phase, Ei is low (high) and the nodes Qi, $\overline{Qi}$, and Si are precharged (predischarged) to VDD (GND). This makes the next gate operated in the precharge phase and the next enable signal is low (high). When Ei raises to high (low), the H-ALCDL (L-ALCDL) circuit is operated in the evaluation phase. There exists a path from one of the output nodes to GND (VDD) while the other path is off. Thus there always exists a small voltage difference between the two output nodes, which causes the sense amplifier to trip. Finally the output nodes with a lower voltage is discharged rapidly to GND (VDD) while the other node remains at VDD (GND). The L-ALCDL is also designed by NMOS differential logic network which is connected to VDD. The full swings of the output signals is generated by the sense amplifier.

When the ECDL is in the evaluation phase, the output nodes exist only one path to VDD, i.e. through the sense amplifier. When the H-ALCDL (L-ALCDL) is in the evaluation phase, there exist two path to GND (VDD), i.e., through the sense amplifier and the NMOS differential logic tree. Simulation results show that the ALCDL has better speed performance and dissipates less power than the ECDL. It is also proved that the ALCDL has good speed performance for complex gates.

Fig. 4(a) (4(b)) shows the N-C^{2}MOS (P-C^{2}MOS) latch for conventional differential logic circuits. Fig. 4(c) (4(d)) shows the new differential N-latch (P-latch). When the clock is low (high), the nodes Qn and $\overline{Qn}$ (Qp and $\overline{Qp}$) are precharged (predischarged) to VDD (GND). When the clock rises (falls), the N-C^{2}MOS (P-C^{2}MOS) latch is turned on. Both output nodes Ln and $\overline{Ln}$ (Lp and $\overline{Lp}$) are pulled low (high) before the input signals arrive. The evaluation operation is completed after the input signals arrive. Thus more power is dissipated due to the extra transition. The timing diagram is shown in Fig. 5(a) (5(b)). The output signals of the new clocking scheme only change states after the input signals are received. There is no extra transitions at the output nodes Ln' and $\overline{Ln'}$ (Lp' and $\overline{Lp'}$). In order to improve the speed performance and solve the ratio logic problem of the N-latch (P-latch) [6], the modified N-latch (modified P-latch) is designed with improved logic network as shown in Fig. 5(e) (5(f)).

III. DESIGN EXAMPLE

The carry-propagation-free multiplier with 4-2 compressor is a regular cellular array structure suitable for high-speed multiplication [7]. The 4-2 compressor can add four conventional binary partial products of the same weights to two bits with the carry propagation. The equivalent circuit of a 4-2 compressor by two serial full adders is shown in Fig. 6(a). The 4-2 compressor is designed with two complex gates which generate the two output bits SUMi and CARRYi. The NMOS differential network is shown in Fig. 6(b). The comparisons of the 4-2 compressors designed by dynamic differential cascode voltage switch (DCVS) logic, ECDL, H-ALCDL, and L-ALCDL are shown in Fig. 7. It is seen that the DCVS is the slowest of all. The ECDL dissipates more power than others. The H-ALCDL is the fastest of all and the L-ALCDL dissipates the least power. As the power supply reduces, the advantages of the H-ALCDL and L-ALCDL can be further seen. Simulation results of 3-, 5-, and 7-input XOR/XNOR differential gates designed by these logic circuits show that the H-ALCDL and L-ALCDL have good speed performance, especially for complex logic.

IV. CONCLUSION

In this paper, a new true-single-phase clocking scheme, is proposed and analyzed. The new clocking scheme is implemented using locally asynchronous logic circuits. In each pipelined section, only the first gate of the asynchronous circuits and the latch stage are controlled by the global clock. Therefore, the clock loading can be reduced and the design of the clock buffer can be eased. During the precharge phase, the locally asynchronous circuits are not simultaneously precharged. Thus the current spike induced by the precharge operation is much reduced. New differential latches are also proposed to prevent the extra transitions and reduce the power dissipation. A 4-2 compressor is designed using the new asynchronous logic circuits. Simulation results show that the new asynchronous circuits have high-speed and low-power performances, especially at low power supply voltage.

REFERENCES

[1] Y. Jiren, I. Karlsson, and C. Svensson, "A true single-phase-clock dynamic CMOS circuit technique," IEEE J. Solid-State Circuits, vol. SC-22, pp.899-901, Oct. 1987.

[2] Y. Jiren and C. Svensson, "High speed CMOS circuit technique," IEEE J. Solid-State Circuits, vol. SC-24, pp. 62-70, Feb. 1990.

[3] G. M. Jacobs and R. Broderson, "A fully asynchronous digital signal processor using self-timed circuits," IEEE J. Solid-State Circuits, vol. SC-25, pp. 1526-1536, Dec. 1990.

[4] S. L. Lu, "Implementation of iterative network with CMOS differential logic," IEEE J. Solid-State Circuits, vol. SC-23, pp. 1013-1017, Aug. 1988.

[5] M. Afghahi and C. Svensson, "Performance of synchronous and asynchronous schemes for VLSI," IEEE Trans. Computer, vol. C-41, pp. 858-872, Jul. 1992.

[6] H. Y. Huang and C. Y. Wu, "Clock-slope-insensitive self-timed DCVS latch (SDL) for true-single-phase CMOS pipelined systems," revised by IEEE Trans. Circuits & Systems, Part II.

[7] J. M. Masato et al., "A 10-ns 54x54 parallel structure full array multiplier with 0.5-um CMOS technology," IEEE J. Solid-State Circuits, vol. SC-26, pp. 600-606, Apr. 1991.

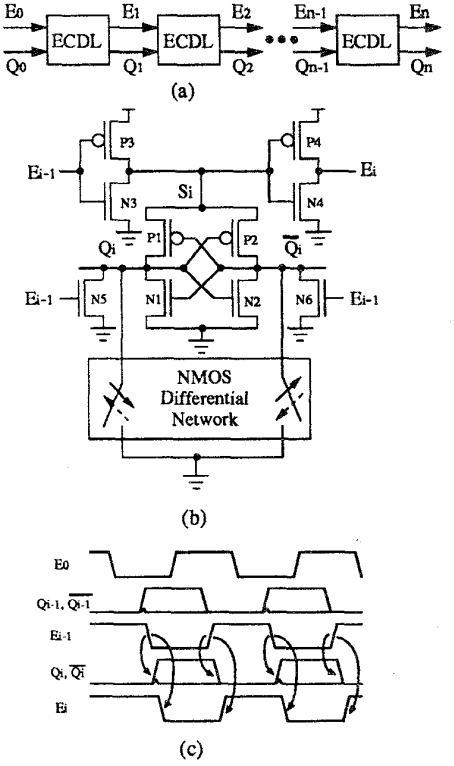

Fig. 2 (a) Block diagram, (b) circuit structure, and (c) timing diagram of the ECDL.

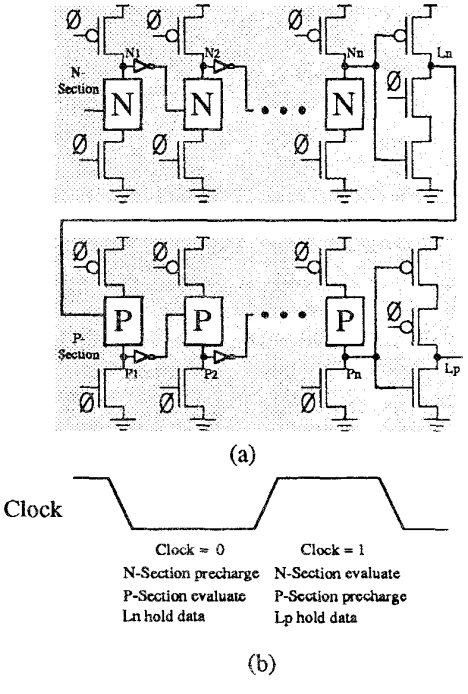

Fig. 1 (a) General circuit structure and (b) clock timing of the conventional true-single-phase clock system.

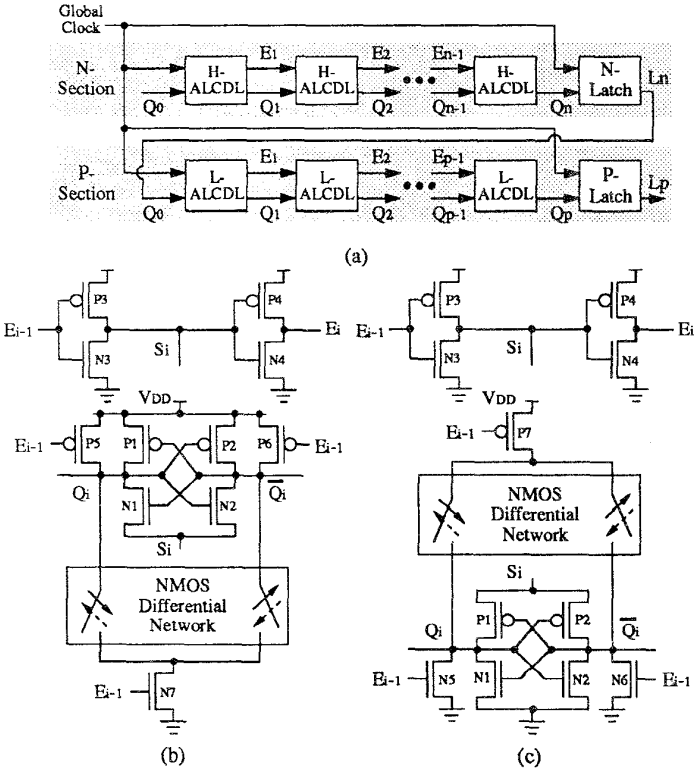

Fig. 3 (a) Block diagram of the new true-single-phase clocking scheme. (b) Circuit structure of H-ALCDL. (c) Circuit structure of L-ALCDL.

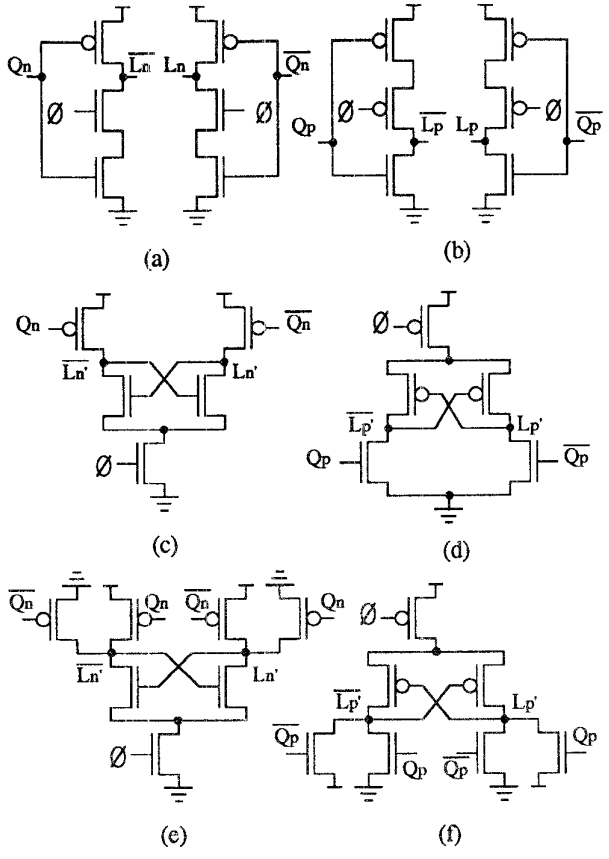

Fig. 4 (a) N-C^{2}MOS latch. (b) P-C^{2}MOS latch. (c) New N-latch. (d) New P-Latch. (e) Modified N-Latch. (f) Modified P-latch.

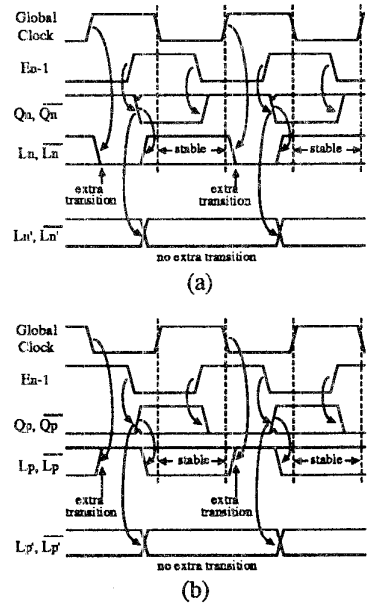

Fig. 5 The timing diagram of (a) N-section and (b) P-section in the new true-single-phase clocing scheme.

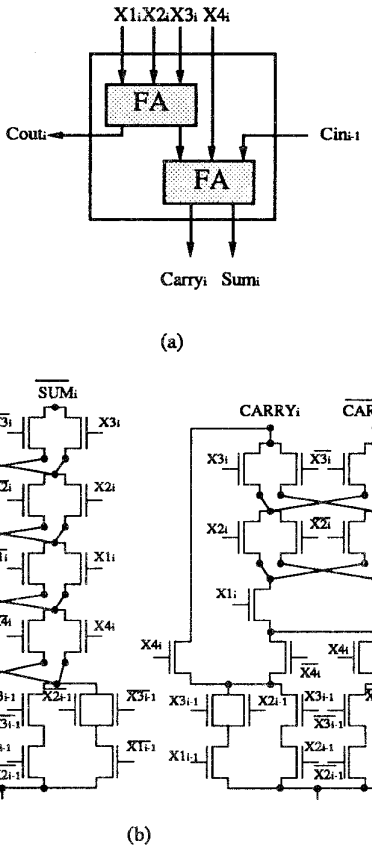

Fig. 6 (a) The equivalent circuit of a 4-2 compressor by two serial full adders. (b) The NMOS differential logic network of the 4-2 compressor.

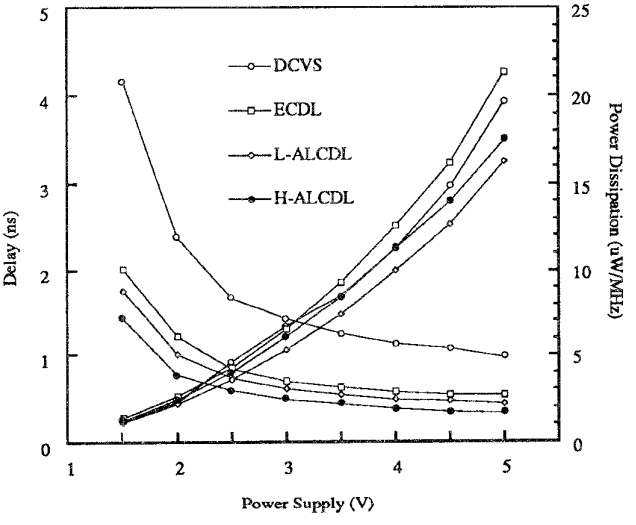

Fig. 7 Comparisons of speed and power dissipation in different power supply voltage.