Low Voltage Low Power High-Speed BiCMOS Multiplier

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Abstract

A 16x16-bit parallel multiplier fabricated in a 1.0-μm BiCMOS technology is described. The chip uses a modified array scheme incorporated with Booth's algorithm to reduce the adding stages of partial products. The combination of CMOS and BiCMOS circuits and advanced arithmetic architecture achieve a multiplication time of 32.74ns while dissipation only 298μW at 2.5V supply voltage operation.

I. Introduction

CMOS and bipolar technology have their characteristics and circuit performance. CMOS circuits have low static power dissipation and high packing density. But, the speed is limited by the capacitive loading. On the other hand, bipolar digital circuits outperform CMOS in terms of speed, but suffered by static power dissipation. There is a performance gap between CMOS circuit and ECL circuit as shown in Fig.1 [1]. It can be achieved by a technology such as BiCMOS to cover the full delay-power space.

A variety of digital BiCMOS circuit structures has been developed [2]–[6]. BiCMOS circuits have demonstrated superior performance over their MOS counterparts because of the high trans-conductance of bipolar transistors. The advantages of these are : I) low static power consumption, II) superior driving capability of on- and off-chip loads, and III) lower delay sensitivity to capacitive loading, which is important especially for semi-custom integrated circuit design. BiCMOS has been exploited at the system level as well. It has been used for fast ECL SRAMs, microprocessors, etc. The availability of CMOS and bipolar devices on the same chip can also be used for mixing slow/low-power and fast/high-power logic families. The high-speed circuits should be used to the critical delay paths only. This strategy allows for efficient management of speed and power.

In this paper, the low-voltage low-power and high-speed multiplier design application of BiCMOS technology to 16x16-bit is shown. The strategies for the low-voltage and high-speed multiplier employing BiCMOS technology are as fellows : I) increase the integration density by using circuits and reduce interchip communications which cause long delay times; and II) accelerate the critical delay path by using bipolar drivers without increasing the total chip size.

II. Low-Voltage and High-speed BiCMOS Circuit

In the multiplier design, two feedback controlled enhanced-pull-down BiCMOS circuit structure for the low voltage low power high speed regime are used [6].

A. *Feedback-Controlled Enhanced-Pull-Down BiCMOS Inverter*

Fig.2 shows the feedback inverter BiCMOS. To achieve a high-speed full-swing operation in BiCMOS circuits, full output-swing operation of bipolar transistors must be realized.

When the input makes low-to-high transition, Q1 is turned off and MP2 continues in the on state for a while duo to the feedback CMOS inverter FBI1. The base current of Q2 is supplied through MP3 and MP2 from VDD. Thus, there is no drain-source and source-gate voltage loss during pull-down operation which achieves and high speed performance under low power supply condition. When the input signal makes a high-to-low transition, MP1 is turned on and Q1 drives the load until output voltage nearly reach VDD-VBE and the feedback CMOS inverter FBI2 brings output to the magnitude of the supply voltage.

B. *Feedback-Controlled Enhanced-Pull-Down BiCMOS Tri-state Buffer*

Fig.3 shows the circuit of the feedback-controlled enhanced-pull-down BiCMOS tri-state buffer. When control signal V_{en} is high and the signal makes a high-to-low transition, MP3 and MP1 are turned off and the excess minority carriers of Q1 are discharge immediately through MN1 when turns off Q1. MP4 remains in the on state for a while due to the feedback CMOS NAND gate NAND1. The base current of Q2 is supplied by MP4 and MP5 form VDD. Thus there is no drain –source and source-gate voltage loss during pull-down operation. When the

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input signal make a low-to-high transition, MP3 and MP6 are turned on and Q1 drives the load until the output voltage nearly reach VDD-VBE, and the MP6 brings the output to the magnitude of the supply voltage.

III. Chip Design

Multiplication arithmetic is usually realized as additions of partial products. Therefore, one of the most important design constraints is reduced the number of additions in order to increase the operation speed. The modified Booth's algorithm is used to reduce the number of partial products and a Wallace tree array scheme is used to reduce the addition stages. A Wallace tree incorporated with a Booth's implementation has been prevailing in high-speed multipliers. However, the Wallace tree suffers from poor structure regularity.

The block diagram of the 16x16-bit multiplier is shown in Fig.4 . The chip consists of a modified Booth's encoder, a modified adder array, and a carry propagation adder. In the multiplier design, modified Booth's algorithm are used to reduce the number of partial products. The modified Booth's algorithm scheme is to consider a bit pair each step, which reduces the number of multilicand's multiples by half per each multiplication this means that only half number of adders are used in an overlapped multiplier-bit scanning design.

This multiplier used a further modified adder array implementing a Booth's algorithm. Fig.5 shows five basis cells which consist of a simple full adder. A modified adder array used the five basic cells to perform two reduction addition stages for the partial product reduction process as shown in Fig.6 . In the first reduction addition stage, different adder combinations are used to reduce the number of partial products to four partial products in each column. Then, the second reduction addition stage use 4:2 adder to reduce the partial products to two 32-bit operands. Using this modified adder array implementing a modify Booth's algorithm, the maximum number of adder stages in a column is reduced to five. Moreover, this array achieves a highly regular cell configuration and affords good design productivity and a short design time.

Fig.7 shows a block diagram of the final carry propagation stage, the carry lookahead adders (CLA's) are fully utilized to speed up the carry propagation in the final stages. The conventional 32-bit adder involves eight 4-bit CLA in series. This worst-case propagation time can be improved by adding the carry bypass circuit to each 4-bit CLA.

III. Simulation Result

The multiplier design using FC-EPD-BiCMOS circuits are separated into three parts as shown in Fig.5. First port is Booth's decoded and encoder. FC-EPD-BiCMOS inverter circuits are used as the out buffers of Booth's encoders to improve the driving capability as shown in Fig.8 .

Second part is a modified adder array used to minimize the critical path gate stages. In order to improve the regularity of Wallace tree structure five types of adder cell are used to simplify the interconnection of adder array. The adder outputs are only connected to only one gate at next addition stage. Thus CMOS circuit technique is used to design the adders.

Third part is a 32-bit CLA with carry bypass circuits as shown in Fig.7. The critical delay path for signal propagation is from the first stage 4-bit CLA which generates C3 and bypassed by six bypass circuits and through the last 4-bit CLA to the sum output. FC-EPD-BiCMOS tri-state buffers are used in the carry bypass circuit of a 32-bit CLA to improve the operation speed. The layout of this design sre shown in Fig. 9.

The HSPICE port-simulation result of the key features of the chip are shown in Table 1 and Table 2. The combination of BiCMOS technology and a modified adder array incorporating a Booth's decoder has achieved a multiplication time of 32.74 ns and a power dissipation of 298μW at 2.5V supply voltage operation.

IV. Conclusion

BiCMOS circuit has been demonstrated to be the better device technology for low power high-speed VLSI's, not only due to its low power dissipation and high density of CMOS transistor, but also due to its high-speed characteristics of bipolar transistor. Design strategies for multiplier employing BiCMOS technology shown that low voltage, low power, and high speed application is possible.

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