A Suggestion for Low-Power Current-Sensing Complementary Pass-Transistor Logic Interconnection

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Abstract

In this paper, a new circuit interconnection scheme of the low-power current-sensing complementary pass-transistor logic (LCSCPTL) is proposed and analyzed. The proposed new circuit scheme using full-swing and non-full-swing output signals to control the NMOS pass transistor logic tree network. Due to the non-full-swing outputs and the current-sensing scheme, the new logic circuit scheme can improve the power dissipation and operation speed. The non-full-swing LCSCPTL is applied to the design of the parallel multiplier. The 4-2 compressors and the conditional carry selection scheme are used in this design to achieve regular layout and improve the operation speed. Moreover, the 1.2V 8*8-bit parallel multiplier can be fabricated without changing the conventional 5V CMOS process. The operation speed of the parallel multiplier is 32 ns for 1.2v supply voltage.

I. Introduction

For low-voltage digital systems the different pass-logic CPL-like styles are promising for low power and high-speed applications. Many logic families and sensing scheme have been proposed to achieve high operation speed and reduce the power dissipation. The latched complementary pass-transistor logic (CPL) [1] as shown in Fig. 1 have been proven to have potential in low power digital circuit design [2].But due to the delivered voltage from NMOS PTL logic tree of the CPL is only Vdd-Vth and the voltage slop is slow. The CPL does not keep the speed and low voltage operation., The CSCPTL circuit as shown in Fig. 2 is proposed [3] to improve the speed performance on low-voltage operation. But the CSCPTL consumes more dynamic power dissipation than the latched CPL. The LCSCPTL circuit [4] has been proposed to reduce the power dissipation and also keep the speed performance. In this paper, an improved circuit scheme of the LCSCPTL, called the non-full-swing LCSCPTL is proposed and analyzed. The 1.2V 8*8-bit multipliers are also given as the various logic circuits design comparisons.

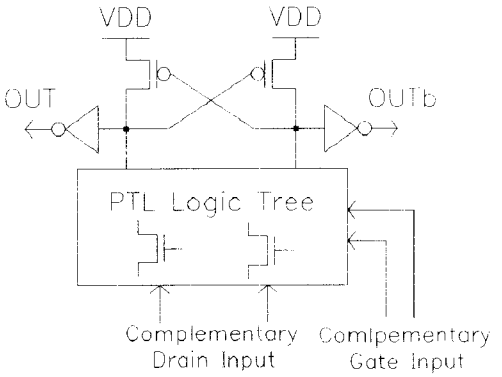

Fig. 1 The circuit diagram of the latched CPL

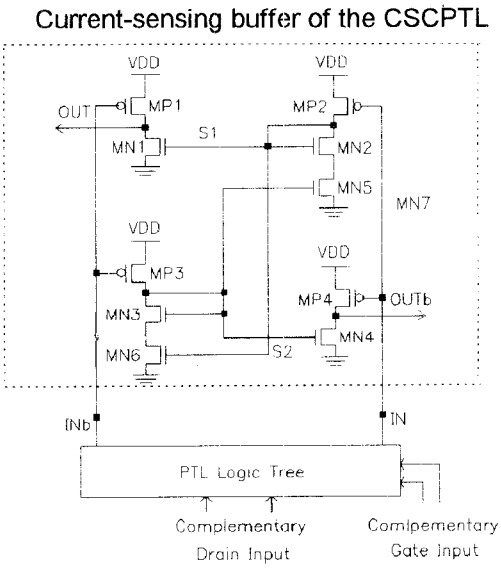

Fig. 2 The circuit diagram of the CSCPTL

II. The LCSCPTL and The Non-Full-Swing LCSCPTL

In the following, the architecture and operative principles of the LCSCPTL circuit and non-full-swing LCSCPTL circuit are shown.

A. The architecture of the LCSCPTL

Fig. 3 shows the current-sensing buffer of the LCSCPTL. The nodes IN and INb are output nodes of the pass-transistor logic tree. The internal nodes S1 and S2 are the cross storage nodes.

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PMOS MP1-MP4 are the transconductance amplifiers which convert voltage to current. MN2 and MN3 are the current-sensing devices. MN1 and MN4 are used to mirror and amplify the sensed current from the PMOS transconductance amplifiers. If INb=1 and IN=0, PMOS MP1 and MP3 will be turned off and MP2, MP4 are turned on. Then node S1 starts to be charged by MP2 and S2 is discharged. MN5 and MN6 are used to cut off the dc current path after evaluation. The NMOS MN7 and MN8 are used as the gate-to-source/drain capacitances, shunted with MN2 and MN3, to reduce the negative feed-back effect of the MOS transistors MN2 and MN3 during logic switching. Thus the switching speed of the nodes S1 and S2 are improved. It also results that the dynamic power dissipation of the LCSCPTL circuit is decreased.

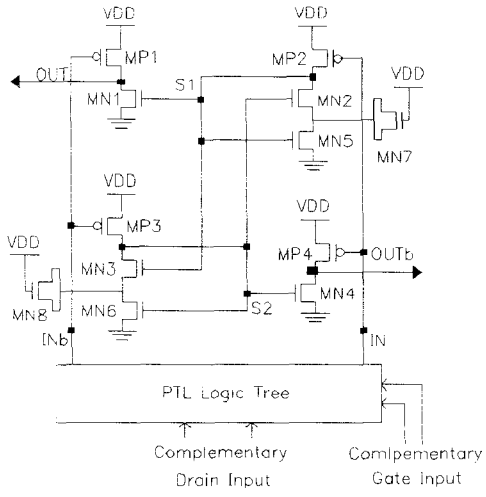

Fig. 3 The LCSCPTL

B. The Non-Full-Swing LCSCPTL

Obviously, the LCSCPTL circuit has the non-full-swing internal nodes S1 and S2 to accelerate the logic switching. The MOS transistor MP1, MN1, MP4 and MN4 are used as the output stage of the LCSCPTL to provide the full-swing output voltage. A new circuit interconnection scheme called non-full-swing LCSCPTL is shown in Fig. 4, where the MOS transistor MP1, MN1, MP4 and MN4 are removed. The nodes S1 and S2 are connected to the OUT and OUTb as the output nodes respectively. It makes the new logic circuit has the non-full output voltages swing from Vtn to VDD. It saves the output stage MOS transistors, hence saves the output stage delay. Moreover, as shown in Fig. 4, the PTL logic tree has two different types of input signals, the complementary drain input and the complementary gate input. By using the non-full-swing output signals as the complementary gate input of the next logic gate to control the Gate of the PTL logic tree. Due to the reduced output voltage swing, it can accelerate the logic gate operation speed and reduce the power dissipation.

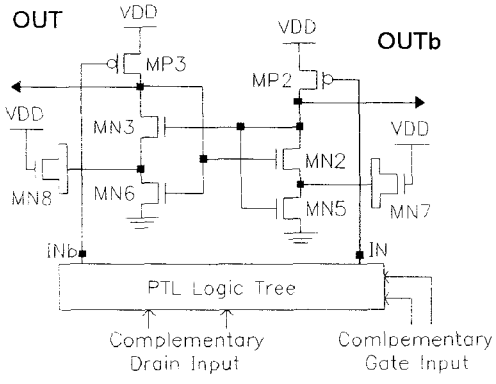

Fig. 4 The non-full-swing LCSCPTL

III. Comparison of the Interconnection in PTL Tree

The PTL logic tree has two different types of input signals, it makes the gate delay comparison is complex. In order to compare the gate delay and power dissipation, the fixed gate connection and fixed drain connection of the pass-transistor logic tree are shown. For example, in the SUM circuit as show in Fig. 5, if the gate signal Y, Yb, Z or Zb is come from the critical delay signal (the longest delay signal), it is called as the fixed drain connection type. On the other hand, if the drain signal X or Xb is come from the critical delay signal to control to outputs , it is called as the fixed gate connection type. Based upon 0.8um CMOS process HSPICE simulation, the gate delay and power dissipation comparison results of the SUM circuit of the CPL, LCSCPTL and non-full-swing LCSCPTL are shown in Fig. 6. Due to the non-full-swing LCSCPTL only can be used as the complementary gate input, thus it has no fixed gate connection type. It is seen that the delay of LCSCPTL is 2.5 times higher than CPL in the fixed gate connection type. In the fixed drain connection type, the non-full-swing LCSCPTL consumes lowest dc power dissipation and least gate delay than other two.

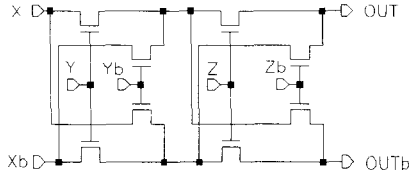

Fig. 5 The pass transistor logic tree of sum circuit

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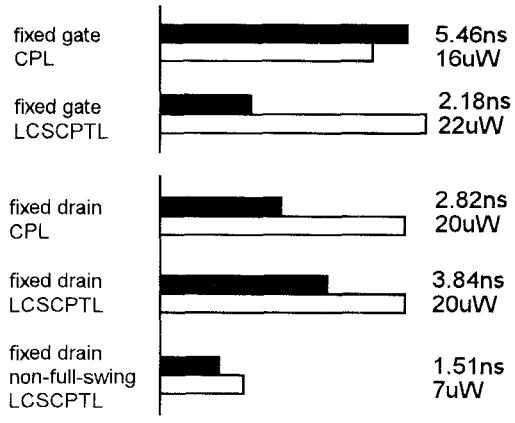

Fig. 6 The sum circuit delay in different logic family and its average power dissipation

IV. Multiplier Architecture

The Baugh-Wooley algorithm [5] is used to achieve the 2's-complement parallel multiplier. The structure of this parallel multiplier as shown in Fig. 7 is divided into two parts. The first part is the partial-product generation and carry-save addition array. The second part is the carry look-ahead adder circuit. Since this multiplier performs 8 * 8-bit multiplication, eight partial products are generated in this case. In order to improve the operational speed of the carry save addition array. The carry save addition array of the eight partial products are divided into two groups, the upper four partial products array and the lower four partial products array. The upper or lower four partial products array can be added into two products by adopting one 4-2 compressor addition stage, and only two 4-2 compressor addition stages are needed to add all the eight partial products into two products. Finally, two products are added with the 12-bit CLA to form the final result. As shown in Fig. 8, the 4-bit conditional carry selection (CCS) [6] [7] is used to implement the 12-bit CLA design. Fig. 9 shows the structure of the 12-bit CLA. The final result is generated by the conditional-sum selection (CSS) circuits. Fig. 10 shows the logic trees of the pass-transistor of the multiplier. They include AND/NAND gate, OR/NOR gate, sum part, carry part, and multiplexers.

V. Simulation Results

The process time of the 8 * 8-bit parallel multiplier by using CPL, LCSCPTL and non-full-swing LCSCPTL is 66.5 ns, 55.6 ns and 31.9 ns individually as shown in Fig. 11. They are based upon the HSPICE simulation results under 1.2V where the threshold voltage of NMOS and PMOS transistors is 0.75V and -0.9V, respectively. Fig. 12 shows the power dissipation comparisons. The power dissipation simulation results are simulated

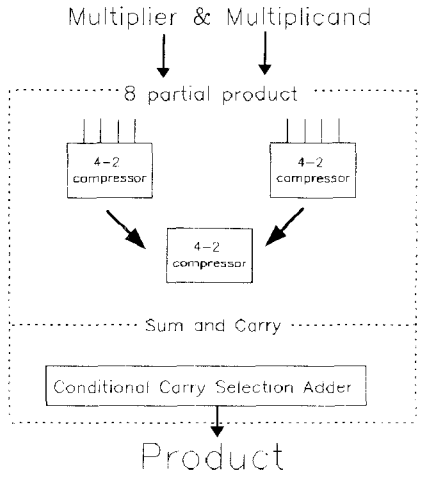

Fig. 7 The Structure of Multiplier

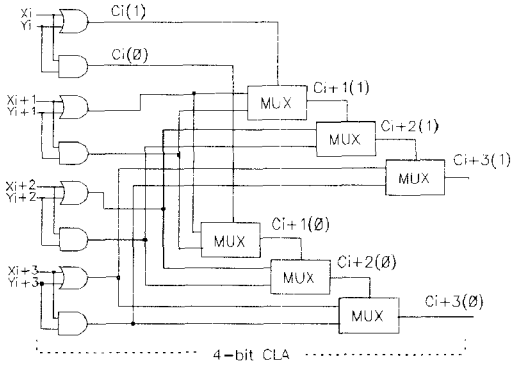

Fig. 8 Conditional Carry Selection (CCS) circuit

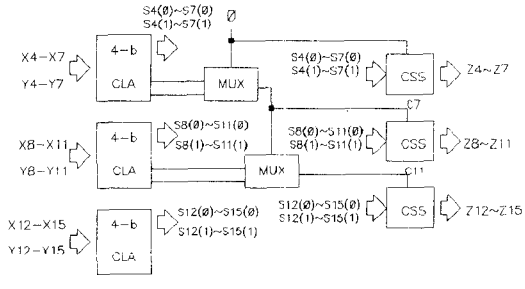

Fig. 9 Block Diagram of the 12-b CLA

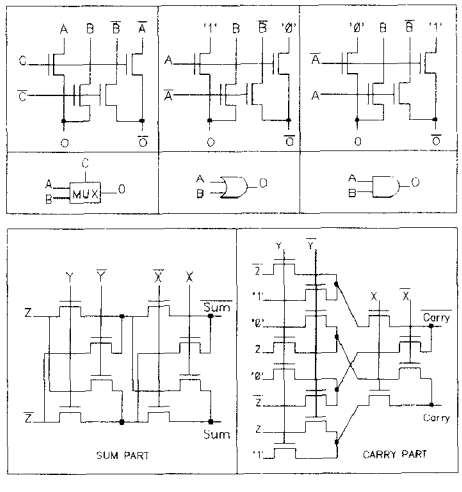

Fig. 10 The Logic Tree of the PTL

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under 20MHz operating frequency. From the simulated results, it is seen that the operation speed of the non-full-swing LCSCPTL is about 2.1 times higher than the latched CPL. Moreover, the non-full-swing LCSCPTL has less power dissipation than the latched CPL. Finally, the characteristics of this multiplier are summarized in Table I.

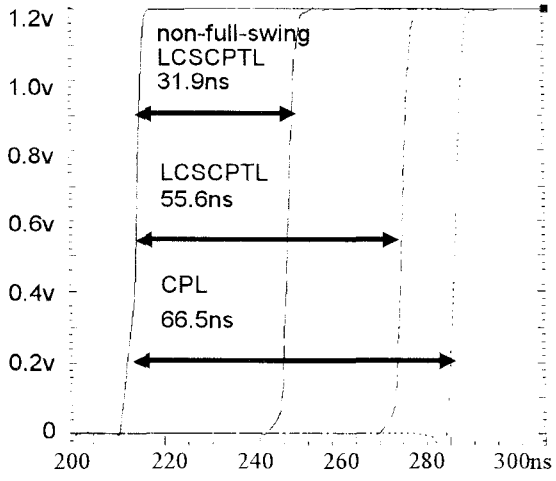

Fig.11 The Process Time of the 8x8 parallel multiplier

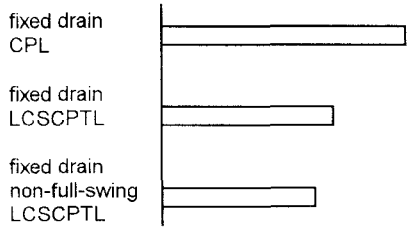

Fig.11 The power dissipation of the 8x8 parallel multiplier

Table I

Process Technology			
MOSFET	gate	length	0.8 um
MOSFET	gate	oxide	19.0 nm
NMOSFET	threshold	voltage	0.75 v
PMOSFET	threshold	voltage	-0.9 v

Experimental Result			
	delay time	power dissipation	power delay product normalized
CPL	66.5 ns	48.1 uW	1
LCSCPTL	55.6 ns	39.6 uW	0.688
non-full-swing LCSCPTL	31.9 ns	35.1 uW	0.349

VI. Conclusion

This paper describes a 1.2V 8 * 8-bit parallel multiplier by using the non-full-swing low-power current-sensing complementary pass-transistor logic (non-full-swing LCSCPTL) circuit. The 4-2 compressors and conditional selection scheme are used in this design to achieve the regular structure of the layout and the fast operation speed. The non-full-swing LCSCPTL circuit is shown has advantages in both speed and power dissipation. In summary, the design of this work are quite promising for low-voltage low-power high speed VLSI applications.

References

[1]Kazuo Yano, Toshiaki Yamanaka, Taksshi Nishida, Masayoshi Saito, Katsuhiro Shimohigashi, and Akihiro Shimizu, "A 3.8ns CMOS 16x16-b Multiplier Using Complementary Pass-Transistor Logic," *IEEE J. Solid-State Circuits,* vol. 25, pp. 388-395, Apr. 1990.

[2]Abdellatif Bellaouar and Mohamed I.Elmasry, "Low-Power Digital VLSI Design: Circuit and Systems," Kluwer Academic publishers, Norwell, MA, 1995.

[3]Chung-Yu Wu, Jr-Houng Lu, and Kuo-Hsing Cheng, "A New CMOS Current-Sensing Complem- entary Pass-Transistor Logic (CSCPTL) for High- Speed Low-Voltage Application," *Proc. of 1995 IEEE ISCAS,* Seattle, U.S.A., May 1995. pp. 25-28.

[4]Kuo-Hsing Cheng, and Yii-Yih Liaw, "A Low-Power Current-Sensing Complementary Pass-Tran- sistor Logic (LCSCPTL) for Low-Voltage High- Speed Applications," *Proc. of 1996 Symposium on VLSI Circuits, Tech. Dig.*, Honolulu, Hawaii, June 1996. pp.16-17.

[5]C. R. Baugh and B. A. Wooley, "A two's complem- ent parallel array multiplication algorithm," *IEEE Trans. Comput.*, vol. C-22, pp. 1045-1047, Dec. 1973.

[6]M. Suzuki, N. Ohkubo, T. Yamanaka, A. Shimizu, and K. Sasaki, "A 1.5 ns 32b CMOS ALU in Double Pass-Transistor Logic," *IEEE ISSCC. Digest of Technical Papers,* pp. 90-91, 1993.

[7]M. Suzuki, N. Ohkubo, T. Shinbo, T. Yamanaka, A. Shimizu, K. Sasaki, and Y. Nakagome, "A 1.5 ns 32b CMOS ALU in Double Pass-Transistor Logic," *IEEE J. Solid-State Circuits,* vol. 28, no. 11, pp. 1145-1150, Nov. 1993.

[8]Kuo-Hsing Cheng* and Liow Yu Yee, "The Design of Low Power Current-Sensing Complementary Pass-Transistor Logic and It's Application for Low-Voltage High-Speed Multiplier" proc. of 1996 IEEE ICECS.

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