A 1.2V CMOS Multiplier Using Low-Power Current-Sensing Complementary Pass-Transistor Logic

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Abstract

This work describes a CMOS 8 * 8-bit parallel multiplier for 1.2V supply voltage. The low-power current-sensing complementary pass-transistor logic (LCSCPTL) is applied to the design of the parallel multiplier. The LCSCPTL have certain advantages in both speed and power dissipation over the CPL circuit. The 4-2 compressors and the conditional carry selection scheme are used in this design to achieve regular layout and improve the operation speed. Moreover, the 1.2V low-voltage 8 * 8-bit parallel multiplier can be designed and fabricated without changing the conventional 5V 0.8 m CMOS process. Based upon the HSPICE simulation results, the operation speed of the parallel multiplier is 54 ns for 1.2v supply voltage.

1. Introduction

In the portable system, micropower integrated circuits play an important role. Generally, power supply scaled-down is the most efficient method to realize power reduction of digital circuits. Apparently, it makes the circuit delay increased. Many logic families and sensing scheme have been proposed to achieve high operation speed and reduce the power dissipation. Several pass- transistor logic families, such as the latched complementary pass-transistor logic (CPL) [1] as shown in Fig. 1 have been proven to have potential in low power digital circuit design [2]. But the CPL does not keep the speed performance on low-voltage operation due to the delivered voltage from NMOS logic tree of the CPL is only Vdd-Vtn, that could be less than 400mV at 1.2V power supply applications. Thus the voltage output slop of the multiple cascaded NMOS logic tree is slow. It also increases the short circuit power dissipation at cross-coupled PMOS latch. In order to improve the speed performance on low-voltage operation, the CSCPTL circuit as shown in Fig. 2 is proposed [3]. But the CSCPTL consumes more dynamic power dissipation than the latched CPL.

In view of those advantages and disadvantages, in this work a 8 * 8-bit 2's complement parallel multiplier for 1.2V supply voltage is proposed and analyzed. In order to improve the operation speed and reduce the power dissipation, the low-power current-sensing complementary pass-transistor logic (LCSCPTL) [4] is applied to the design of the parallel multiplier. Based upon the HSPICE simulation results, the operation speed of the parallel multiplier is 54 ns for 1.2V supply voltage. Moreover, the fabrication technology of this work is the conventional 5V 0.8 um CMOS process.

2. LCSCPTL

The LCSCPTL has two mutually compatible version. They are described below:

2.1. The First Version of the LCSCPTL

Fig. 3 shows the current-sensing buffer of the first version of the LCSCPTL. In Fig. 3, the nodes IN and INb are output of the pass-transistor logic tree. The nodes S1 and S2 are the cross storage nodes. PMOS transistors MP1-MP4 are the four single-transistor transconductance amplifiers which convert voltage to current. MN2 and MN3 are the current-sensing devices. MN1 and MN4 are used to mirror and amplify the sensed current from the PMOS transconductance amplifiers. If INb=1 and IN=0, PMOS MP1 and MP3 will be turned off and MP2, MP4 are turned on. Then node S1 starts to be charged by MP2 and S2 will be discharged when MN6 (controlled by the node S1) is turned on. MN5 and MN6 are used to cut off the dc current path after evaluation. Obviously, if the nodes S1 and S2 cab be transferred state quickly, it will improve the short circuit power dissipation. In order to accomplish this target, the MOS transistors MN7 and MN8 are inserted in the master part of the sense-amplifier. The MOS transistors MN7 and MN8 are used as the gate-to-source/drain capacitances. Because the NMOS transistors MN2 and MN3 result in the negative feedback effect, the switching speed will degrade. By adding the capacitors MN7 and MN8, shunted with MN2 and MN3, the negative feed-back effect can be reduced during switching, and the switching speed is improved. It also results that the dynamic power dissipation of the LCSCPTL circuit is decreased.

2.2. The Second Version of the LCSCPTL

Fig. 4 shows the second version of the LCSCPTL. The gates of the NMOS transistors MN2 and MN3 are connected to the output nodes OUTb and OUT, respectively. If IN=0 and INb=1, PMOS MP2 and MP4 will be turned on and MP1, MP3 are turned off. Then the node S1 starts to be charged by the MP2. Since the gate voltage of the MN3 is controlled by the node OUT and keeps in high level at last state. If the node S1 is charged above 0.75V, MN6 will be turned on. Then the

node S2 can be discharged until the voltage of the node OUT is below 0.75V. Because the nodes S1 and S2 have less capacitive load and the capacitors MN7, MN8 are shunted with MN2, MN3. The switching speed of the nodes S1 and S2 are improved. But careful design is needed when the output nodes have different capacitive load.

The LCSCPTL circuits have certain advantages in speed and power dissipation due to that all the internal nodes are limited voltage swing. It makes the logic states of the internal nodes can be transferred quickly. Thus the MOS transistors of the LCSCPTL current-sensing buffer can be turned on or turned off quickly. In this way, it also makes the dynamic power dissipation is reduced effectively.

3. Multiplier Architecture

In this work, the Baugh-Wooley algorithm [5] is used to achieve the 2's-complement parallel multiplier. The structure of this parallel multiplier as shown in Fig. 5 is divided into two parts. The first part is the partial-product generation and carry-save addition array. The second part is the carry look-ahead adder circuit. Since this multiplier performs 8 * 8-bit multiplication, eight partial products are generated in this case. In order to improve the operational speed of the carry save addition array. The carry save addition array of the eight partial products are divided into two groups, the upper four partial products array and the lower four partial products array. The upper or lower four partial products array can be added into two products by adopting one 4-2 compressor addition stage, and only two 4-2 compressor addition stages are needed to add all the eight partial products into two products. After the addition of two 4-2 compressor stages, it will generate a 12-bit sum and carry. Finally, the 12-bit sum and carry are added with the 12-bit CLA to form the final result. As shown in Fig. 6, the 4-bit conditional carry selection (CCS) [6] [7] is used to implement the 12-bit CLA design. Fig. 7 shows the structure of the 12-bit CLA. Obviously, the final result can be generated by the conditional-sum selection (CSS) circuits. The CSS circuit consists of multiplexers that select the conditional sums, Sj(0) or Sj(1), according to the incoming block carry signal.

The whole logic gates of the multiplier are implemented by the first version of the LCSCPTL circuit. Fig. 8 shows the logic trees of the LCSCPTL. They include AND/NAND gate, OR/NOR gate, sum part, carry part, and multiplexers.

4. Simulation Results

The critical gates of the 4-2 compressor or the conventional full adder are the multi-input XOR gates. The speed comparisons on multi-input XOR gates of the CPL, the CSCPTL, the first version LCSCPTL, and the second version LCSCPTL are shown in Fig. 9. They are based upon the HSPICE simulation results where the threshold voltage of NMOS and PMOS transistors are 0.75V and -0.9V, respectively. Fig. 10 shows the power dissipation comparisons. The power dissipation simulation results are simulated under 40MHz operating frequency and 1.2V supply voltage. From the simulated results, it is seen that the operation speed of the LCSCPTL is about 2.2 to 2.6 times higher than the latched CPL. Moreover, the LCSCPTL has less power dissipation and the more the logic complexity is, the more the circuit performance benefit of the LCSCPTL is.

The process time of the 8 * 8-bit multiplier is 54 ns as shown in Fig.11. It is also based upon the HSPICE simulation results under 1.2V. The characteristics of this multiplier are summarized in Table I.

5. Conclusion

This paper describes a 1.2V 8 * 8-bit parallel multiplier using the low-power current-sensing complementary pass-transistor logic (LCSCPTL) circuits. The 4-2 compressors are used in this design to achieve the regular structure of the layout and the fast reduction of the partial products. The conditional carry selection scheme is used to improve the speed of the final addition. Moreover, the LCSCPTL circuits have certain advantages in both speed and power dissipation over other conventional pass-transistor logic circuits. In summary, the design of this work are quite promising for low-voltage low-power high speed VLSI applications.

References

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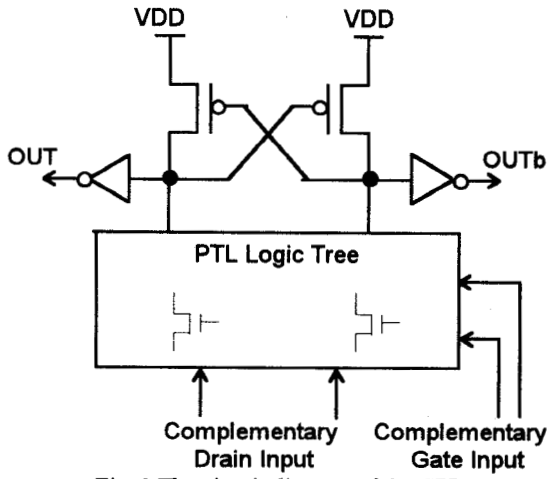

Fig. 1 The circuit diagram of the CPL

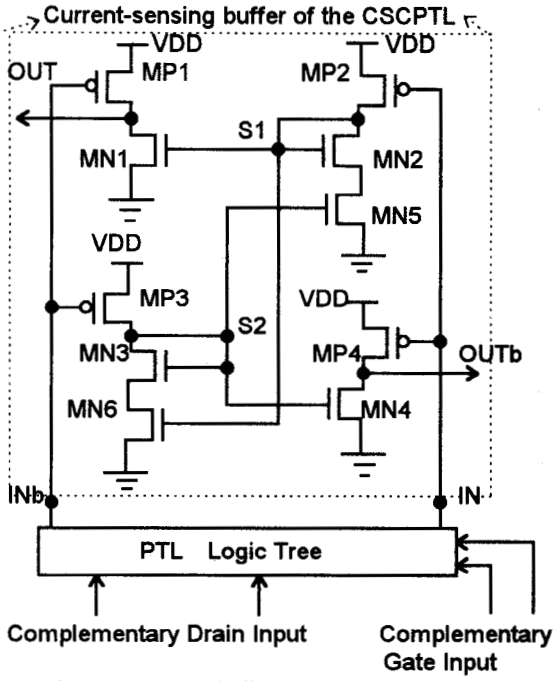

Fig. 2 The circuit diagram of the CSCPTL

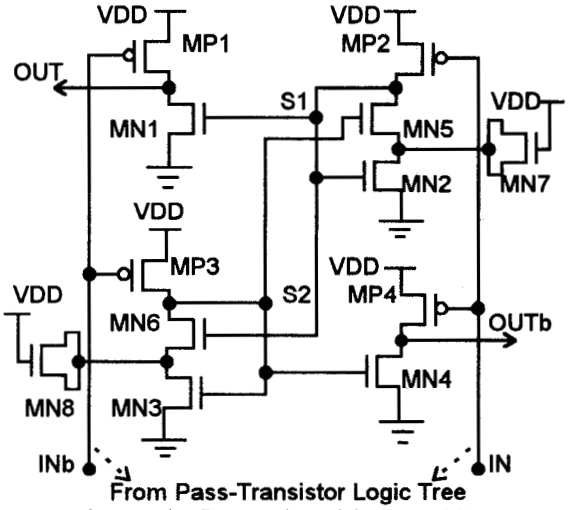

Fig. 3 The first version of the LCSCPTL

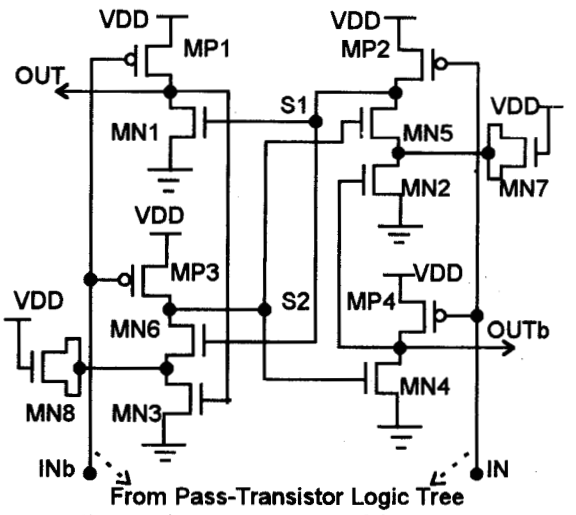

Fig. 4 The second version of the LCSCPTL

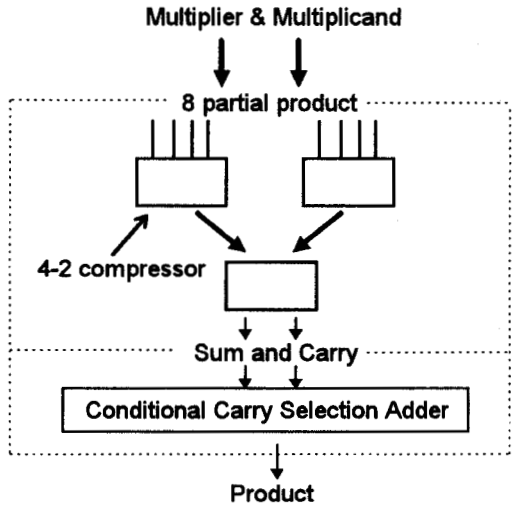

Fig. 5 Structure of multiplier

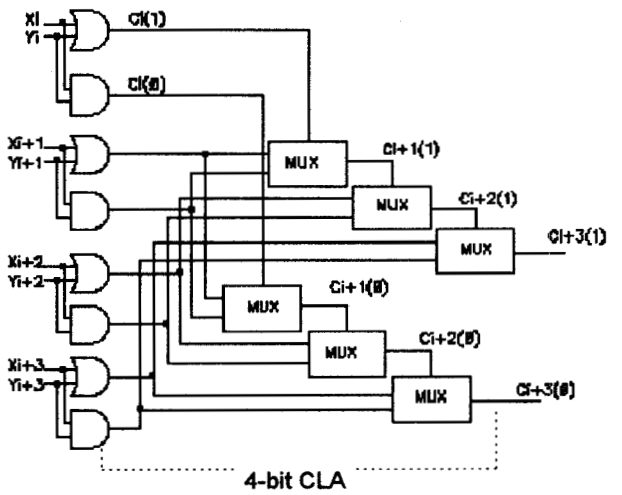

Fig. 6 Conditional carry selection (CCS) circuit

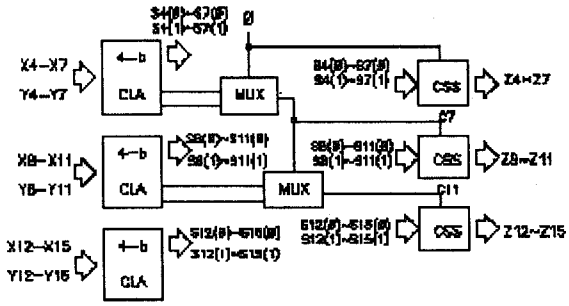

Fig. 7 Block diagram of the 12-b CLA

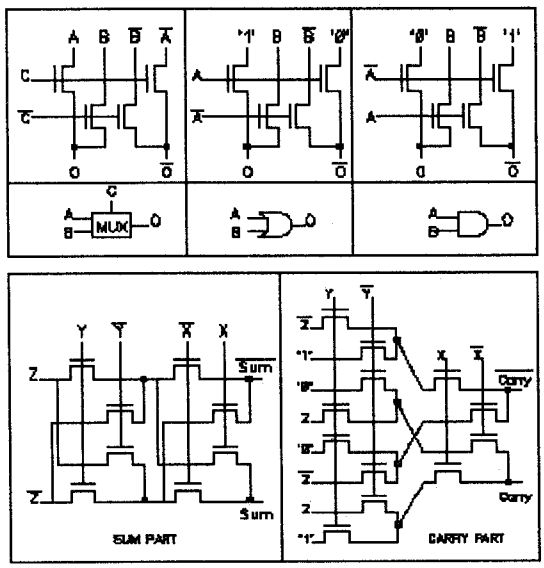

Fig. 8 The logic tree of the LCSCPTL

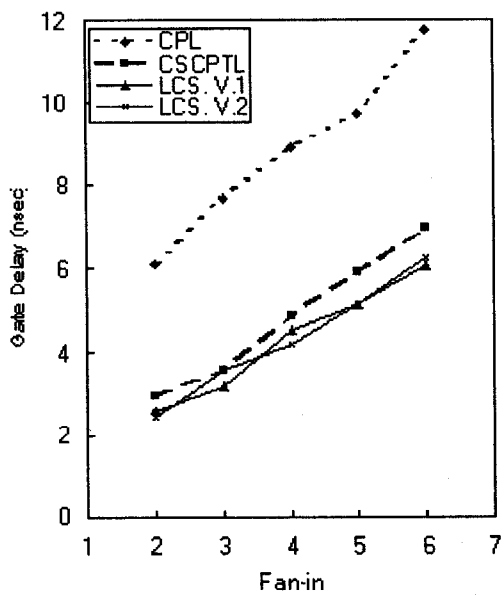

Fig. 9 The gate delay comparisons of the XOR/XNOR gates

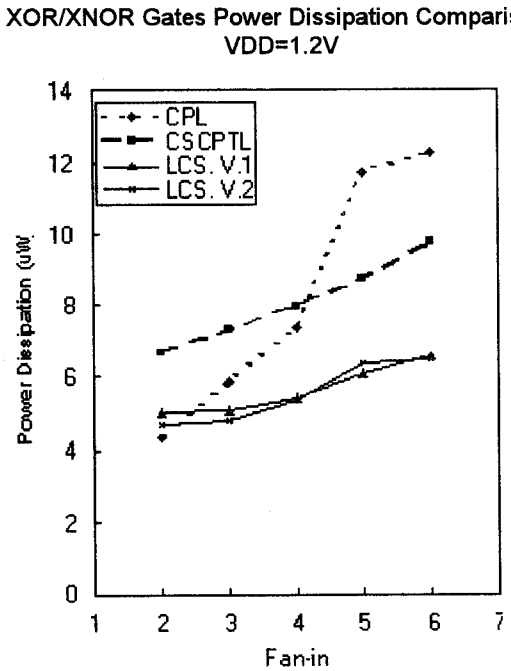

Fig. 10 The power dissipation comparisons of the XOR/XNOR gates

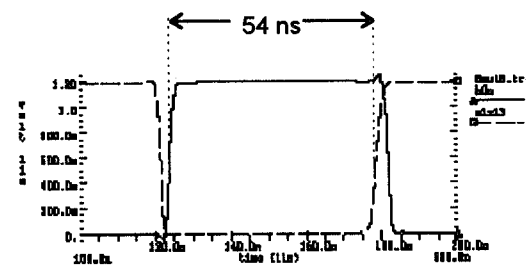

Fig. 11 The process time of the 8 x 8 parallel multiplier

TABLE I.
Characteristics of the 8 x 8-bit Multiplier

Organization	8 x 8-bit MUL (with sign)
Product	16 bit (with sign)
Circuit	LCSCPTL+CCS CLA
Multiplication time	54 nsec
Power at 18 MHz	0.276 mW
Supply Voltage	1.2V