A DIFFERENCE DETECTOR PFD FOR LOW JITTER PLL

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ABSTRACT: For high speed and low jitter PLL application, a new phase frequency detector (PFD) with difference detector is proposed. Because the proposed difference detector PFD (dd-PFD) doesn't have any feedback path in phase frequency detector circuit, it can be operated up to 1.6GHz. Furthermore, with difference detector, the dd-PFD has three-state, so it will not have phase errors and jitter problems. The dead zone of dd-PFD is 16ps. The proposed PFD is designed using 0.35um CMOS technology at 3.3V power supply.

1. INTRODUCTION

Phase Locked Loop (PLL) can be used for data transmission systems and mobile communication systems. As shown in Fig. 1, the PLL consists of five blocks: a phase frequency detector (PFD), a charge pump (CP), a loop filter (LF), a voltage-controlled oscillator (VCO) and a frequency divider (FD). A PFD can monitor the difference between the Ext_f clock and the Int_f clock. It generates an Up signal if the Ext_f clock leads the Int_f clock and a Down signal if the Ext_f clock lags the Int_f clock. The output node voltage Vc of the CP is charged or discharged controlled by Up and Down. Furthermore, a loop filter can filter high frequency noise, and produce a voltage Uf to control the output frequency of the VCO.

A conventional PFD (con-PFD) is shown in Fig. 2. The con-PFD has large dead zone in phase characteristics at the steady state, which generates a large jitter in locked state in PLL. Also, a large amount of power consumption cannot be avoided in high frequency operations because internal nodes of the con-PFD are not completely pull up or pull down. Furthermore, the maximum speed of the con-PFD is limited by the critical path, which is shown in Fig. 2. Because the con-PFD is an asynchronous state machine, the delay time to reset all internal nodes slows down the circuit speed. The critical path forms a feedback path with six gate delays. It limits the speed of the con-PFD. Another PFD, the non-clocked PFD (nc-PFD) proposed for higher frequency application is shown in Fig. 3. The nc-PFD has no dead zone characteristic, because its architecture is very simple and doesn't have any feedback path. However, the nc-PFD has a four-state output. As shown in Fig. 8, if the PLL is locked, Up and Down signals rise to high at the same time. This may cause many problems. Moreover, its phase characteristic depends on a duty cycle of input signals. Thus, the nc-PFD has phase errors and jitter problems, and these will be discussed later.

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In this paper, a new PFD is proposed which can work at a higher frequency. Moreover, our proposed PFD has a three-state output and it will not have phase errors and jitter problems like nc-PFD.

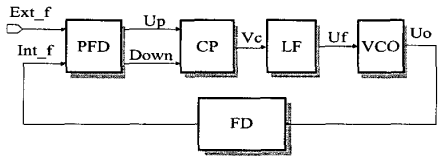

Fig. 1 PLL Architecture

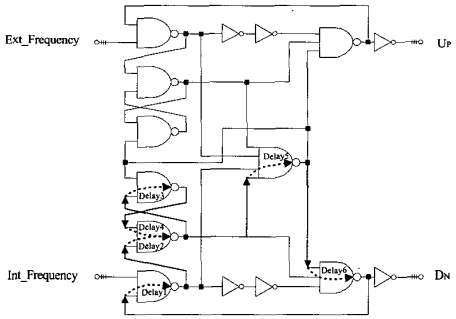

Fig. 2 The schematic of con-PFD

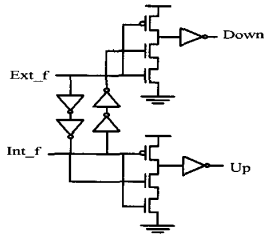

Fig. 3 The schematic of nc-PFD.

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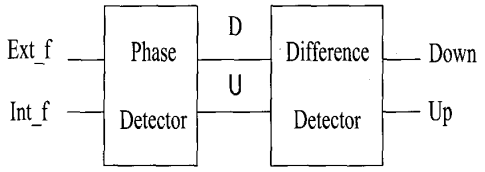

Fig. 4 The proposed new PFD block diagram

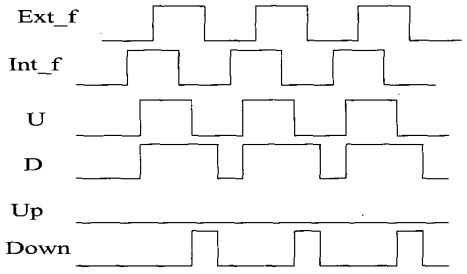

Fig. 5 Waveforms for the case when Int_f leads before the Ext_f signal.

2. CIRCUIT STRUCTURE AND OPERATING PRINCIPLE OF THE PROPOSED PFD

As shown in Fig.4, the proposed new PFD has two basic blocks, the phase detector and the difference detector. The input clock signals Ext_f and Int_f are used to generate the intermediate output signals U and D. Final output signals Up and Down used to control the charge pump are the pulse width difference of the intermediate output signals. As shown in Fig. 5, only a pulse of the Down signal is generated, and it equals to the difference of the pulse widths U and D. The detail transistor schematics and operating principles of the phase detector and the difference detector are shown as following:

2.1 Phase detector circuit

The schematic of the proposed new four-state phase detector is shown in Fig. 6 (a). The inverter delay chains and the NAND gates are used as the edge detection circuits of the input clock signals. The pulse signals of the internal nodes Rd, Sd and Su are corresponding to the negative edge of the input clock signal Ext_f, the negative edge of the signal Int_f and the positive edge of the signal Int_f. Because the edge detection circuits have the same logic depth, we can make pulse signals Rd, Sd and Su respond to variety of the input clock signals at the same time. It can avoid generating dead-zone between input clock signals. Waveforms and operating principle of the new four-state phase detector are shown in Fig. 6 (b).

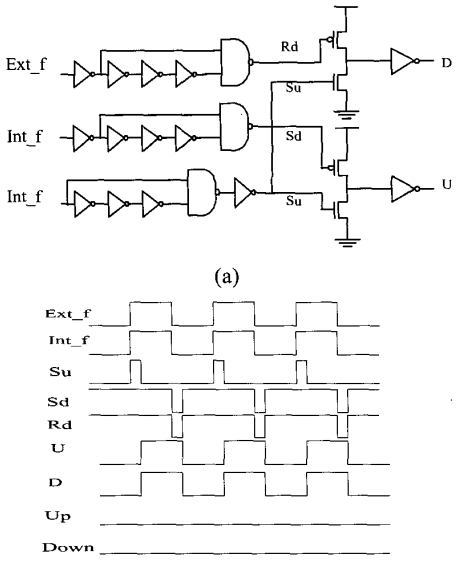

Fig. 6 (a) The schematic of the proposed new four-state phase detector. (b) Waveforms of the proposed new PFD.

If the Ext_f signal's up-edge arrives, the U and D signals are not affected. If the Int_f signal's up-edge arrives, the U and D signals are from low to high. But, if the Int_f signal's down-edge arrives, the U signal is from high to low and the D signal is not affected. If the Ext_f signal's down-edge arrives, the D signal is from high to low and the U signal is not affected. In other words, if U and D signals stay low, and the Ext_f signal's up-edge arrives, they remain at low level. If Int_f signal's up-edge arrives, U and D signals are from low to high.

2.2 Difference detector circuit

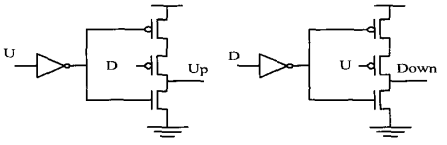

Fig. 7 Difference Detector circuit

The proposed new four-state PFD and the four-state nc-PFD show the simplest structure, thus they can be used for high frequency application. But the nc-PFD has current mismatch and jitter problem shown as following. When the Int_f signal has the same frequency and phase with the Ext_f signal, the intermediate output signals U and D of proposed new four-state PFD and the output signals Down and up of nc-PFD shown in Fig. 6 (b) and Fig. 8 have the same pulse width.

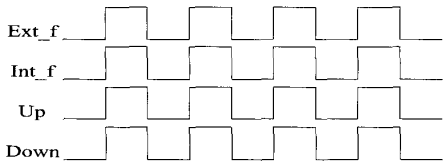

Fig.8 Waveforms of the nc-PFD is shown when Int_f has the same frequency and phase with Ext_f.

In this situation, we must have the same charging and discharging currents in the charge pump controlled by the output of four-state PFD to maintain the lock-in phase. However, it is difficult task due to nonideal effect of the MOS transistors. It will cause the mismatch of the charging and discharging current in the charge pump. For example, a different VDS voltage in the charging current path will cause the current mismatch due to channel length modulation effect. Moreover, as shown in Fig. 9, the periodic charging and discharging controlled by the output of the nc-PFD will cause the jitter problem in the charge pump output.

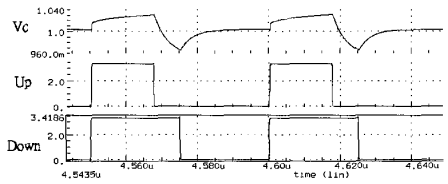

Fig. 9 Output of charge pump (Vc), Up and Down signals of the nc-PFD.

Based upon the simulation result, if a 6% mismatch exists in the charging and discharging currents, which a PLL circuit has, the nc-PFD will cause a 13% phase error between the input clock signals Ext_f and Int_f.

Due to the problem shown as previous, the difference detector circuit, in Fig. 7, is used to generate a pulse, which is equal to the pulse width difference of the intermediate signals U and D. The timing diagram is shown in Fig. 6 (b). If the input signals Ext_f and Int_f have the same frequency and phase, we can get the all-zero output signals Up and Down. Due to the difference detector circuit, the new PFD output signals Down and Up have a three-state property. It can avoid the current mismatch problem in the charge pump. Moreover, it doesn't have the periodic charging and discharging on node Vc when the input clock signals Ext_f and Int_f are locked by the PLL.

3. SIMULATION AND COMPARISON RESULTS

A maximum operation frequency definition is one over the shortest period with correct Up and Down signals when the inputs clock signals have the same frequency and 90 degree phase difference. An example of how the maximum frequency varies with the supply voltage is shown in Fig. 10. We can find that the maximum frequency of con-PFD is lower than the dd-PFD. Furthermore, the dead-zone of the dd-PFD is lower.

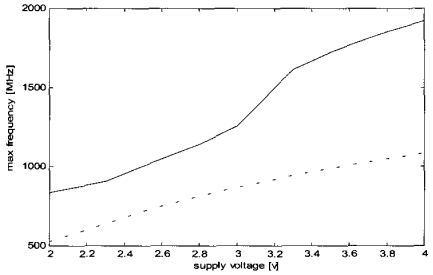

Fig.10 Maximum frequency as function of supply voltage for the dd-PFD (solid line) and con-PFD (dashed line).

A dead-zone occurs when the loop is in a lock mode and the output of the charge pump does not change for small changes in the input signals at the PFD. The dead-zone for different frequencies are plotted in Fig. 11. For the con-PFD, the dead-zone is larger than the dd-PFD, because the dd-PFD does not have to have the feedback path, but the con-PFD does. Thus it is difficult to reduce the dead-zone of the con-PFD. Moreover, a large dead-zone will translate to a large jitter directly in the PLL. This will cause PLL to become unstable.

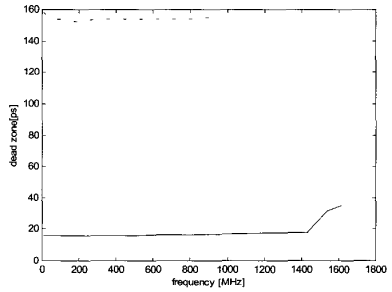

Fig. 11 The width of the dead zones of the dd-PFD (solid) and con-PFD (dash) as function of frequency. The supply voltage is 3.3 V.

The Fig. 12 shows the phase characteristic of the dd-PFD and con-PFD. The dd-PFD has 16ps dead-zone, as shown in Fig. 13, and the con-PFD has 158ps dead-zone. It can be observed that Phase sensitivity of the dd-PFD is linear. But Phase sensitivity of the con-PFD has a changeless region. In addition, the nc-PFD has constant offset in phase characteristics. The nc-PFD has various phase offsets caused by the duty cycle of input signals. This is a

great disadvantage of the nc-PFD. However, the dd-PFD does not have this problem. Moreover, the maximum frequency of the dd- PFD can be operated more than 1.6GHz. In order to understand the lock-in process, we simulate the PLL with the dd-PFD. Fig. 14 shows the lock-in process and Fig. 15 shows output signals of PLL when PLL is locked.

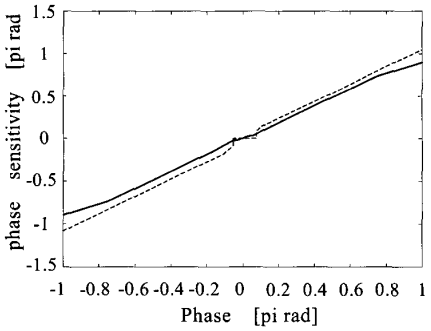

Fig. 12 Phase characteristics of the dd-PFD (solid line) and con-PFD (dashed line) from Hspice simulations, VDD = 3.3 V and f = 200 MHz.

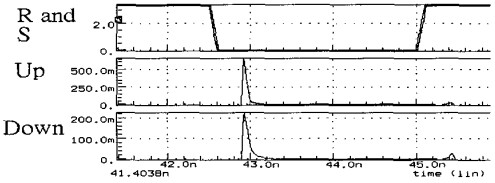

Fig. 13 When the R (Ext_f) signal leads before the S (Int_f) signal 16ps, the dead-zone of the dd-PFD is minimum and only the voltage of Up is higher than Vt.

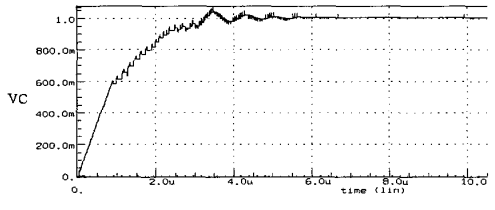

Fig. 14 The lock-in process of a 3–order PLL with the dd-PFD as the phase frequency detector.

4. CONCLUSION

The presented PFD circuit structure is simple and has no feedback paths in the phase detector, thus it can operate up to 1.6GHz in 0.35-um CMOS with a 3.3-V power supply. Without feedback paths, the dead zone of the dd-PFD is very small and jitter will be reduced. Furthermore, with the difference detector, the output state of the dd-PFD will change from four-state to three-state. This property can improve the phase stability significantly when the PLL is locked.

Fig. 15 Output signals are several times the frequency of the Ext_f signal, when PLL is locked. The frequency of the Ext_f signal is 20 MHz and the PLL is 8 times the frequency of the Ext_f signal.

The simulation results of PLL	
Power Supply	3.3V
PFD dead-zone	16ps
CMOS Process	0.35um 1P4M
VCO Frequency Range	80MHz~653MHz
The maximum frequency of Divider	1GHz
PLL consumption	3.3mW~6.5mW
PLL locked range (8 times frequency)	10MHz~82MHz

Table 1. The simulation results of PLL

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