A LOW-POWER HIGH DRIVING ABILITY VOLTAGE CONTROL OSCILLATOR USED IN PLL

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ABSTRACT

Modern high speed CMOS processors using on-chip phase-locked-loops often require a clock buffer with stringent specifications on the signal's rise time and fall time rather than on the buffer's delay time. For these applications we propose a novel voltage controlled oscillator (VCO) with split path CMOS driver. It can be proposed to reduce the total power consumption and phase errors of the PLL. The proposed VCO with the split-path CMOS driver has low power consumption and lower area requirement than that achievable by the traditional tapered CMOS buffer.

I. INTRODUCTION

Phase-locked loop (PLL) is the component broadly used in various field of integrated circuits. The Phase-locked loop is generally used in clock recovery of communication system and frequency synthesizer of wireless communication system. Recently, owing to the broadly use of the mobile electronic systems, low power consumption has become more important in the modern VLSI design. In most applications, the PLL need to connect with other subsystems so it will need buffer to driver the capacitive load. If the capacitive load is too heavy, the power dissipation of the driving circuit will take a large portion of the total power consumption[1]-[5].
In this paper, we use the split-path CMOS driver [7] to reduce power dissipation of the driving circuit and propose a novel VCO to reduce the power consumption of the PLL.

II. The Operation Principle of PHASE-LOCKED LOOP

A block diagram of a simple digital phase-locked loop is shown in Fig. 1. At first, the PFD begins to detect the phase error between the reference signal Ext_f and the feedback signal Int_f. The digital signals UP and DOWN of the PFD output control the VCO through the charge pump (CP). The loop-filter (LF) can filter the high frequency noise and hold the voltage of the node Uf within PLL locked. The frequency divider (FD) is sometimes placed in the feedback loop to make the VCO multiply frequency of the reference signal Ext_f[7][8].
The linear model of this PLL is shown in Fig. 2[9]. The variables $\theta 1$ and $\theta 2$ are the phase of the reference signal Ext_f and the feedback signal Int_f. The parameter K0 is the gain of VCO, and N is the divisor of the frequency divider. The close-loop transfer function H(s) is

$$H(s) = \frac{\omega_n^2 + 2\zeta\omega_n s}{s^2 + 2\zeta\omega_n s + \omega_n^2} \quad (1)$$

ωn is the nature frequency, and ζ is the damping factor.

III. LOW POWER VCO DESIGN

A. *The Source of Power Consumption*

Fig. 3 is the general VCO block which contains the delay Cells. When VCO is oscillating at high frequency, the dynamic power consumption is large due to the large capacitive load. When VCO is oscillating at low frequency, the short -circuit power consumption of the delay cells of VCO will be large.
The main power consumption is produced by the short circuit of every delay cell at transition time. As shown in Fig. 4, when the input is between (VDD-|Vtp|) and Vtn , the PMOS and NMOS will be switched on at the same time. This makes short current flow from VDD to VSS. The period of the short current is longer, the power consumption is larger. To reduce the power consumption, we have to reduce the transition time when the input is between (VDD-|Vtp|) and Vtn or avoid the current flow from VDD to VSS directly.

B. *Low Power VCO with split-path driver*

As shown in Fig. 5, we propose a novel low power VCO to reduce the short circuit power consumption. In this architecture three inverters feedback to oscillate, the Vin signal controls the speed of the charge and the discharge current to adjust the VCO operation frequency. There is no short-circuit power dissipation in C^2-inverter because the waveform-shaper produces the delay time to avoid the current flow from VDD to VSS directly in C^2-inverter part.

C. *Delay pull-high operation*

In Fig 6,when the initial condition is that f=0, delay=0, and out=0, the PMOS transistor M1 and M2 are turned on and the node out rises from 0 to 1. The voltage of the node "Slp" will quickly discharge from 1 to 0 to turn off the NMOS transistor M11. The voltage of the node "Sln" will discharge from 1 to 0 slowly, because the discharge current through the NMOS transistor M6 is limited by the NMOS transistor M7 during

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the node delay pull-high operation.

D. *Delay pull-low operation*

In Fig. 7, when the initial condition is that f=1, delay=1, and out=1, the NMOS transistor M3 and M4 are turned on and the node out falls from 1 to 0. The voltage of the node "Sln" will quickly charge from 0 to 1 to turn off the PMOS transistor M12. The voltage of the node "Slp" will charge from 0 to 1 slowly, because the charge current through the PMOS transistor M9 is limited by the PMOS transistor M8 during the node delay pull-low operation.
Thus the short circuit power dissipation of the VCO self and the succeeding driving buffer is reduced.

E. *The operation of new low-power driver*

We proposed a new waveform shaping circuit that use in split-path CMOS buffer to produce a tri-stated time in node bp and bn. The short-circuit power dissipation of the output inverter will be eliminated by the tri-stating the driver node momentarily before output signal transition. The NMOS transistor M6 and M7 are in series hence the discharge current is smaller then charge current, in the same reason M8 and M9 are in series so that the discharge current is bigger then charge current. We can use of this characteristic to generate nonoverlap signal to avoid short-circuit current of the driving circuit. The result is that the output PMOS transistor MP is always turned off before the NMOS transistor MN is turned on, and similarly the output NMOS transistor MN is always turned off before the output PMOS transistor MP is turned on. The periods when both output transistor are off (tri-stated) are indicate in Fig.8 by the darkened lines.

IV. SIMULATION AND COMPARATION RESULTS

The Hspice simulation results are based upon TSMC 0.35um 3.5V DPDM CMOS process with a 2.5V supply voltage. Fig. 9 is the simulation waveform of the nodes f, delay, and out. The voltage of the node delay is high enough to turn off the PMOS transistor M1 before the voltage of the node f turns on NMOS transistor M3 during the out pull-low operation. The node delay becomes 1 or 0 to turn off M1 or M4 in time so that the short circuit current is eliminated during the charge or discharge period of the node out. The voltage of the node delay is low enough to turn off the NMOS transistor M4 before the voltage of the node f turns on PMOS transistor M2 during the out pull-high operation.
The simulation waveform of the nodes Sln, Slp, Bn, Bp, and Driver are shown in Fig.10. The operation frequency range of low-power VCO with capacitive load CL=100pF is shown in Table.1. As shown in Table.2, when the load CL=100pF, the power consumption of our proposed VCO with split-path driver is smaller than the traditional VCO about 10%. Because the traditional VCO with taper buffer has short-circuit current, it will cause large power dissipation. Our circuit avoids the short-circuit current of driving buffer hence the power dissipation is reduced. The Table.3 is the simulation results of the PLL with proposed VCO.

V. CONCLUSION

In this paper, a low power VCO with split-path CMOS driver and PLL have been proposed and analyzed. The low-power VCO is used in the PLL circuit. According to the simulation result, the low power high driving VCO is saving power over 10% in comparison to conventional VCO. The proposed VCO has two features: (1) no short-circuit current (2) the VCO can shorten the output transition time to reduce the short circuit current of the next stage. We use new waveform shaping circuit in split-path driver to reduce power dissipation of driving circuit. Thus it is suitable for being used in modern low power processors when the clock capacitive load is heavy.

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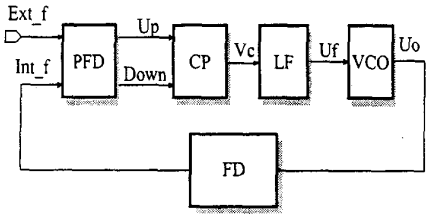

Fig.1 PLL function block diagram

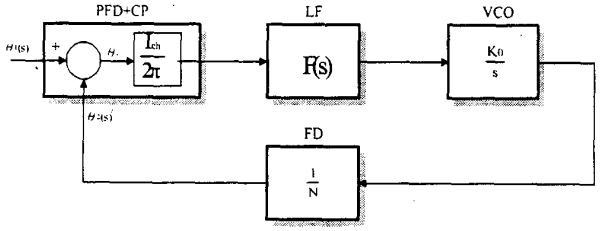

Fig.2 PLL linear model transfer function

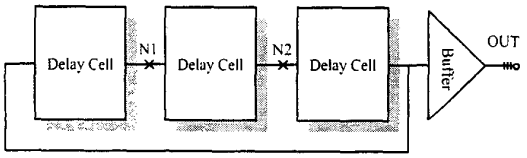

Fig.3 The general VCO Block

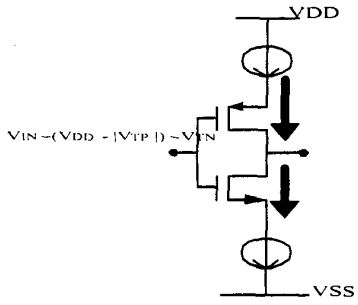

Fig.4 The short current

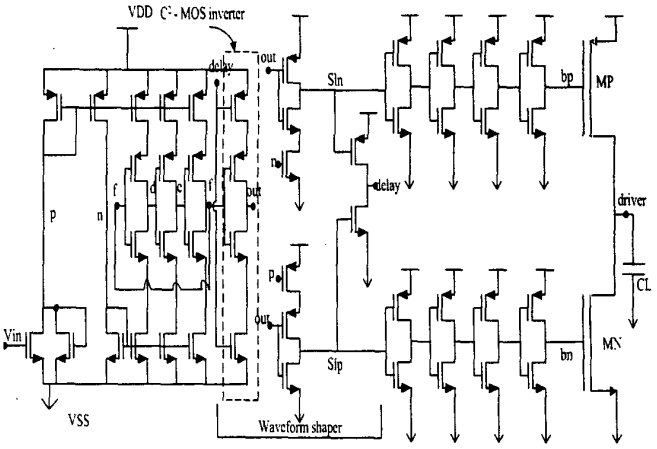

Fig.5 The proposed VCO with split-path driver

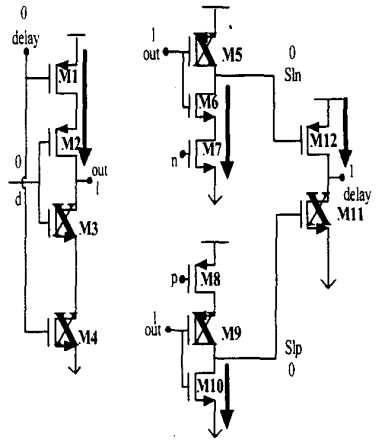

Fig.6 The Charge Period

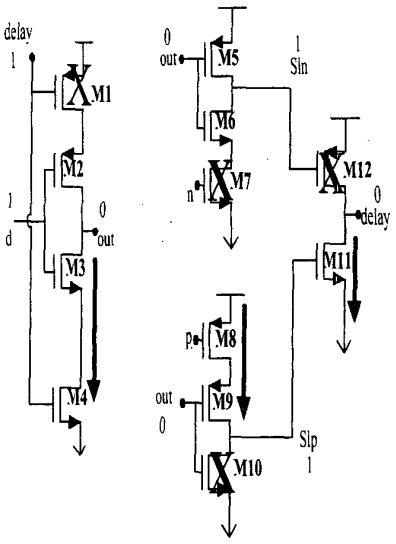

Fig.7 The Discharge Period

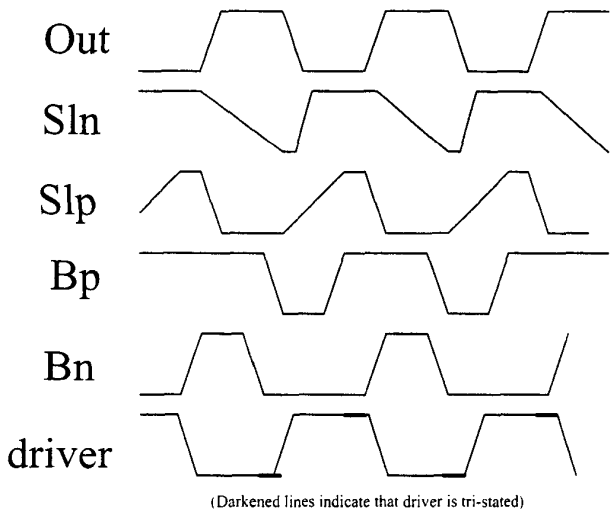

Fig.8 The timing diagram of split-path driver

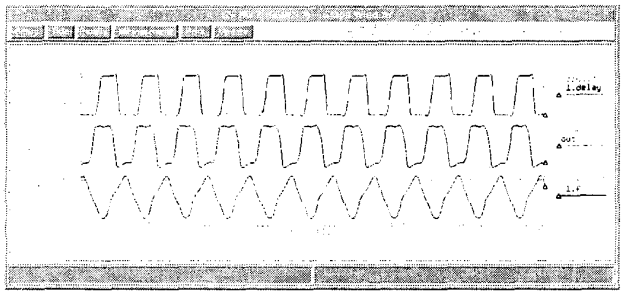

Fig.9 The simulation waveform of delay, out, f

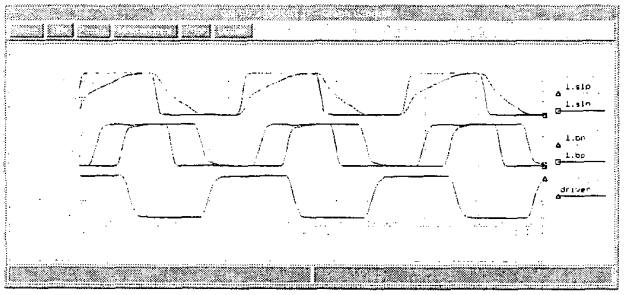

Fig.10 The simulation Waveform of Sln, Slp, Bn, Bp, Driver

Table.1 The simulation of low-power VCO with capacitive load 100p

Vin(V)	Frequency(MHz)	Power(mw)
0~0.4	92.8	81.5
0.6	101.3	88.5
0.8	188.9	167
1.0	299.9	259
1.2	385.7	328
1.4	440.1	371
1.6	474.5	389
1.8	492.8	397
2.0	503.4	399
2.2	509.3	401
2.4	512.1	401
2.5	514.9	404

Table.2 Comparison of power dissipation (mw)

	LOW POWER VCO WITH SPLIT-PATH DRIVER	Ring VCO With Traditional Buffer
Frequency Range (MHz)	92.8~514.9	78~479
Tune Range (MHz)	422.1	401
Max. Power (mw)	404	440
Mini. Power (mw)	81.5	72
mw/100Mhz	76.4	87.2
Avg.gain (Mhz/V)	169.2	160.4

Table.3 The simulation results of PLL with proposed VCO

Locked Freq.(Mhz)	Locked-Time (us)	Long-term-Jitter (ps)	Cycle-Jitter (ps)
300	6	124	60
400	6.5	100	60
500	6.9	112	45