2.2

A Low-Power Current-Sensing Complementary Pass-Transistor Logic (LCSCPTL) for Low-Voltage High-Speed Applications

Kuo-Hsing Cheng*, and Yii-Yih Liaw#

Dept. of Electrical Engineering, Tam-Kang University, Taipei Hsien, Taiwan, R.O.C.
TEL : 886-2-6215656 Ext 731 FAX : 886-2-6221565
EMAIL : cheng@ee.tku.edu.tw* mlii@ee.tku.edu.tw#

Abstract

Recently, power dissipation is becoming an important constraint in portable electronic systems. In this work, a new low-power current-sensing complementary pass-transistor logic (LCSCPTL) is proposed and analyzed. Since the current-sensing scheme can yield a fast sensing speed under small voltage swing than the voltage-sensing scheme, the new logic circuit can be used in the low-voltage low-power digital system for high speed applications. It is shown that the LCSCPTL has an operation speed about 2.2 to 2.6 times higher than the CPL, which is known to have a great potential in low-voltage low-power digital applications. Moreover, the LCSCPTL has less power dissipation than the CPL. These feature make the LCSCPTL very promising in the applications of low-power low-voltage high-speed applications. The LCSCPTL can be operated at 1.2V without changing conventional 5V CMOS process.

Introduction

Recently, low-voltage low-power integrated circuits are essential in portable electronic systems. The portable systems especially personal communication systems will require more and more complicated signal processing. In fact, power dissipation is becoming an important constraint in a design [1] [2]. Thus high performance low-voltage low-power complicated VLSI chips should be developed to satisfy the desideratum.

One way to reduce the power dissipation is to reduce the power supply voltage. It also slows down the circuit operation speed significantly. Therefore, it is the challenge to retain high speed performance under low-voltage, particularly when the power supply voltage approaches the threshold voltage.

The complementary pass-transistor logic (CPL) as shown in Fig. 1 is recognized to have the potential on low-voltage digital circuit design among pass-transistor logic family [3]. The CSCPTL circuit as shown in Fig. 2 is proposed for high-speed application [4]. It is two times faster in gate delay as compared with the CPL. But the CSCPTL consumes more dynamic power dissipation than the CPL. Therefore, the power-delay product of the CSCPTL is similar to the CPL.

In view of the advantages and disadvantages, a new low-power current-sensing complementary pass-transistor logic (LCSCPTL) is proposed and analyzed.

Circuit Techniques

The LCSCPTL has two mutually compatible versions which can be used in the same chip to optimize the system. They are described below:

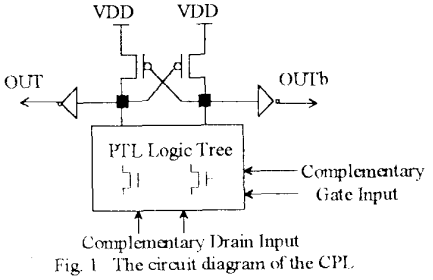


Fig. 1 The circuit diagram of the CPL

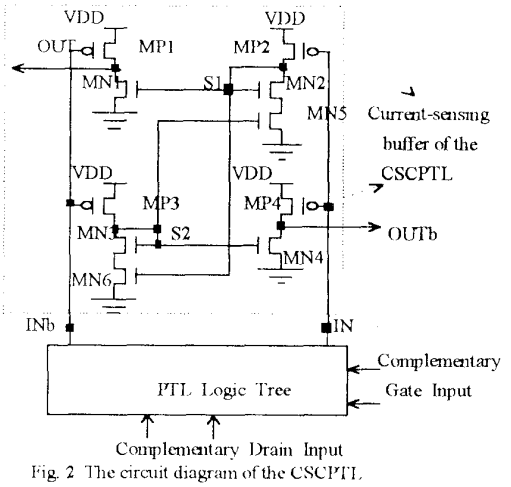
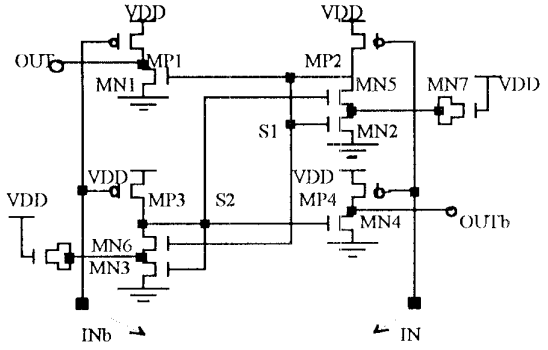


Fig. 2 The circuit diagram of the CSCPTL

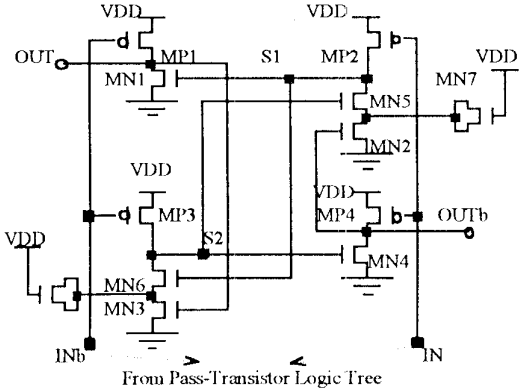
A. The First Version of the LCSCPTL

Fig. 3 shows the current-sensing buffer of the first version of the LCSCPTL. In Fig. 3, the nodes IN and INb are output of the pass-transistor logic tree. The nodes S1 and S2 are the cross storage nodes. PMOS transistors MP1-MP4 are the four single-transistor transconductance amplifiers which convert voltage to current. MN2 and MN3 are the current-sensing devices. MN1 and MN4 are used to mirror and amplify the sensed current from the PMOS transconductance amplifiers. MN5 and MN6 are used to cut off the dc current path after evaluation. The MOS transistors MN7 and MN8 are used as the gate-to-source/drain capacitances. Because the NMOS transistors MN2 and MN3 result in the negative feedback effect, the switching speed will degrade. By adding the capacitors MN7 and MN8, shunted with MN2 and MN3, the negative feed-back effect can be reduced during switching, and the switching

 0-7803-3339-X/96/$5.00©1996 IEEE



From Pass-Transistor Logic Tree
Fig. 3 The first version of the LCSCPTL



From Pass-Transistor Logic Tree
Fig. 4 The second version of the LCSCPTL

speed is improved. It makes the dynamic power dissipation of the LCSCPTL circuit is decreased.

B. The Second Version of the LCSCPTL

Fig. 4 shows the second version of the LCSCPTL. The gates of the NMOS transistors MN2 and MN3 are connected to the output nodes OUTb and OUT, respectively. Thus the nodes S1 and S2 have less capacitive load and the switching speed of the nodes S1 and S2 are improved. But careful design is needed when the output nodes have different capacitive load.

Performance Comparisons

Fig. 5 shows the layout of the CPL, CSCPTL, and LCSCPTL. Based upon 5V 0.8 μm CMOS technology and 1.2 power supply voltage. The speed comparsions on multi-input NAND gates of the CPL, the CSCPTL, the first version LCSCPTL, and the second version LCSCPTL are shown in Fig. 6(a). They are based upon the HSPICE simulation results where the threshold voltage of NMOS and PMOS transistors are 0.75V and -0.9V, respectively. Fig. 6 (b) shows the power dissipation comparsions. The power dissipation simulation results are simulated under 20MHz operating frequency. From the simulated results, it is seen that the operation speed of the LCSCPTL is about 2.2 to 2.6 times higher than the CPL. Moreover, the LCSCPTL has less power dissipation and the more the logic complexity is, the more the circuit performance benefit of the LCSCPTL is.

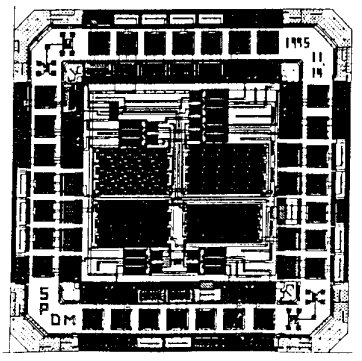


Fig. 5 The layout of the testing circuit

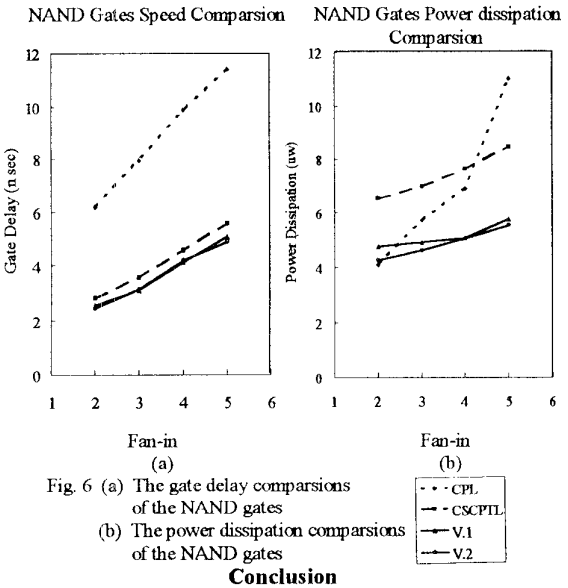


Fig. 6 (a) The gate delay comparsions of the NAND gates
(b) The power dissipation comparsions of the NAND gates

Conclusion

In this paper, a low-power current-sensing complementary pass-transistor logic (LCSCPTL) is proposed and analyzed. The LCSCPTL has two circuit version. It is shown that the LCSCPTL have certain advantages in both speed and power dissipation over the CPL circuit. Thus the LCSCPTL circuits are quite promising for low-voltage high speed VLSI applications.

References

[1] Anantha Chandrakasan, Andy Burstein and Robert. W. Broderson, "A Low-Power Chipset for Portable Multimedia Applications," in Proceedings: IEEE 1994 International Solid-State Circuit Conferen- ce, pp. 82-83, and pp. 31, 1994.

[2] Abdellatif Bellaouar and Mohamed I. Elmasry, "Low-Power Digital VLSI Design: Circuit and Systems," Kluwer Academic publishers, Norwell, MA, 1995.

[3] Kazuo Yano, Toshiaki Yamanaka, Taksshi Nishida, Masayoshi Saito, Katsuhiro Shimohigashi, and Akihiro Shimizu, "A 3.8ns CMOS 16x16-b Multiplier Using Complementary Pass-Transistor Logic," IEEE J. Solid-State Circuits, vol. 25, pp. 388-395, Apr. 1990.

[4] Chung-Yu Wu, Jr-Houng Lu, and Kuo-Hsing Cheng, "A New CMOS Current-Sensing Complementary Pass-Transistor Logic (CSCPTL) for High-Speed Low-Voltage Application," Proc. of 1995 IEEE ISCAS, Seattle, U.S.A., May 1995. pp. 25-28