A CMOS Low Power Voltage Controlled Oscillator With Split-Path Controller

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ABSTRACT

In this paper, the low power VCO is proposed and analyzed. A novel low power voltage controlled oscillator (VCO) is proposed to reduce the total power consumption of the Half-Digital Phase Locked Loop (HDPLL). By Hspice simulation results, the power-frequency ratio of low-power VCO can be reduced over 30% in comparison to conventional VCO. Thus, the novel low power VCO can be used in the low power HDPLL.

1. INTRODUCTION

Phase-locked loop (PLL) is the component broadly used in various fields of integrated circuits. Phase-locked loop is generally used in clock recovery of communication system and frequency synthesizer of wireless communication system [1][2]. Recently, owing to the broadly use of the mobile electronic systems, low power consumption has become the main concern in the modern VLSI design. With the progress of VLSI technology, phase locked loop is necessarily designed in system on a chip [3][4][5]. Thus, PLL has wide applications as well as operational amplifier does. Power consumption has become the main concern in modern VLSI because of the popular use of portable electronics. The goal of the paper is to design a low power phase-locked loop.

In the conventional digital phase- locked loop, PLL contains Phase Detector [6][7], Charge Pump [8], Low Pass Filter, Voltage Controlled Oscillator and Frequency Divider. Voltage controlled osci- llator usually consumes a large portion of power in PLL, thus it is necessary to design a low power voltage-controlled oscillator.

2. DIGITAL PHASE-LOCKED LOOP OVERVIEW

A block diagram of a simple digital phase-locked loop is shown in Fig. 1. At first, the PFD begins to detect the phase error between the reference signal U1 and feedback signal U2. The digital signals of PFD output control the VCO through the charge pump (CP). The loop-filter (LF) can filter the noise and the high-frequency part of output signal of the CP and hold in lock. The frequency divider (FD) is sometimes placed in the feedback loop to make the VCO multiply frequency of the reference signal U1. The linear model of this HDPLL is shown in Fig. 2. The variables θ_1 and θ_2 are the phase of the reference signal U1 and feedback signal U2. The parameter K_0 is the gain of VCO, and N is the divisor of the frequency divider. The close-loop transfer function H(s) is

$$H(s) = \frac{\omega_n^2 + 2\zeta\omega_n s}{s^2 + 2\zeta\omega_n s + \omega_n^2} \quad (1)$$

ω_n is the nature frequency, and ζ is the damping factor.

3. LOW POWER VCO DESIGN

3.1 The source of power consumption

As shown in Fig. 3, the delay cells are contained in the general VCO block. When VCO is oscillating at high frequency, the dynamic power consumption will be large due to the large load capacitance. When VCO is oscillating at low frequency, the short -circuit power consumption of the delay cells of VCO will be large.

The main power consumption is produced by the short circuit current of every delay cell at transition time. As shown in Fig. 4, when the input is between (VDD-|Vtp|) and Vtn , the MOS transistor PMOS and NMOS will be switched on at the same time. The short circuit current will flow from VDD to VSS. The period of the short circuit current is longer and the power consumption is larger. To reduce the power consumption, we have to reduce the transition time when the input signal is between (VDD-|Vtp|) and Vtn or avoid the short circuit current flow form VDD to VSS directly.

3.2 Low power VCO with split-path controller

In Fig. 5, we propose a novel low power VCO to reduce the short circuit power consumption. As shown in Fig. 5, three inverters feedback to oscillate,

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the Vin controls the speed of charge and discharge to adjust the operation frequency. After the node A, there is no short circuit current in the output part and the output transition time is improved.

3.3 Out pull-high operation

In Fig. 6, the initial condition is A=1, F=0 and out=0. When the voltage of the node A falls from 1 to 0, the node out rises from 0 to 1, the PMOS transistor M1 and M2 are quickly turned on and the node out rises from 0 to 1. The voltage of the node "E" will quickly discharge from 1 to 0 to turn off the NMOS transistor M11. The voltage of the node "D" will discharge from 1 to 0 slowly, because the discharge current through the NMOS transistor M6 is limited by the NMOS transistor M7 during the out node out pull-high operation. Due to this, there is no short circuit current in the split-path controller. After the voltage of the node F rises from 0 to 1, the PMOS transistor M1 turns off and NMOS transistor M4 turns on in the output stage. Thus, there is no short circuit current flowing from VDD to VSS directly during output pull-low operation.

3.4 Output pull-low operation

In Fig. 7, the initial condition is A=0, F=1, and out=1.when the voltage of the node A rises from 0 to 1, the node out falls from 1 to 0, the NMOS transistor M3 and M4 are quickly turned on and the node out falls from 1 to 0. The voltage of the node "D" will quickly charge from 0 to 1 to turn off the PMOS transistor M10. The voltage of the node "E" will charge from 0 to 1 slowly, because the charge current through the PMOS transistor M9 is limited by the PMOS transistor M8 during the node out pull-low operation. Due to this, there is no short circuit current in the split-path controller. After the voltage of the node F falls from 1 to 0, the PMOS transistor M1 turns on and NMOS transistor M4 turns off in the output stage. Thus, there is no short circuit current flowing from VDD to VSS directly during out pull-high operation.

Therefore, the short circuit power dissipation of the low power VCO self and the succeeding driving buffer is reduced during the output pull high and pull low operation.

4. CHIP LAYOUT AND SIMULATION RESULTS

The Hspice simulation results are based upon UMC 0.5um DPDM CMOS process with a 3V supply voltage. Table1 shows the simulation results of conventional ring VCO and low power VCO with succeeding output buffer under various control voltage (Vin). Under the same operation frequency, the power dissipation of the proposed low power VCO is lower than the conventional VCO. Table2 show the comparison results of the two VCO. The power-frequency ratio of low-power VCO can be reduced over 30% in comparison to conventional ring VCO. Table3 shows the simulation results of the HDPLL under the various operation frequencies. The long-term jitter is worst because the single-ended architecture is used in the proposed low power VCO. The waveform of low power VCO is shown in Fig. 8. After the node A, the waveform is adjusted to reduce the short circuit current in the output node. The chip layout of the HDPLL is shown in Fig. 9.

5. CONCLUSION

In this paper, the low power VCO and HDPLL have been proposed and analyzed. The chip of proposed HDPLL is implemented with 0.5um CMOS process technology. The layout area of the chip is $0.32\times 0.47mm^2$. The long-term jitter is worst because the single-ended architecture is used in the proposed low power VCO. The proposed low power VCO has two features: (1) no short circuit current. (2) the low power VCO can improve the output transition time to reduce the short circuit current of the succeeding stage. The power-frequency ratio of low-power VCO can be reduced over 30% in comparison to conventional ring VCO.

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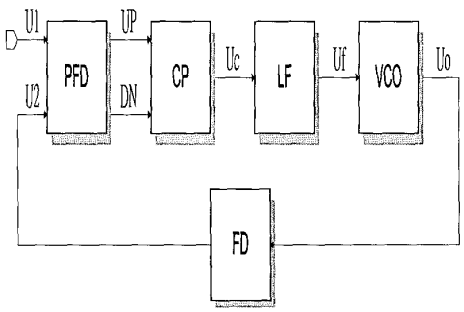


Fig. 1 HDPLL function block diagram

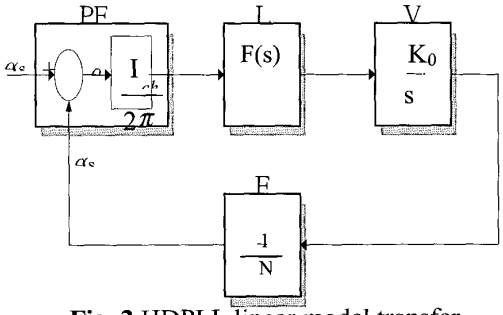


Fig. 2 HDPLL linear model transfer

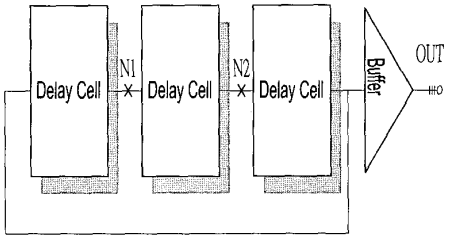


Fig. 3 The general VCO Block

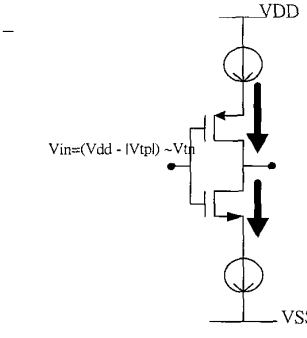


Fig. 4 Short circuit current

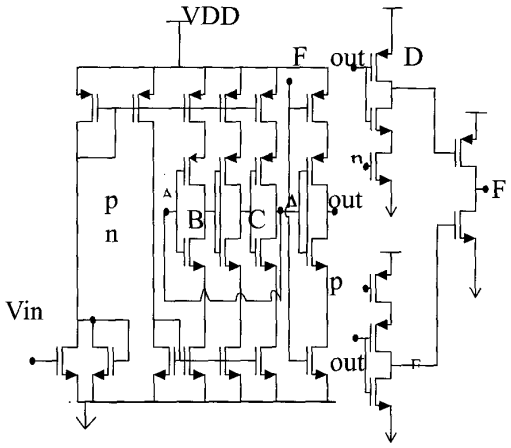


Fig. 5 The proposed of low power VCO

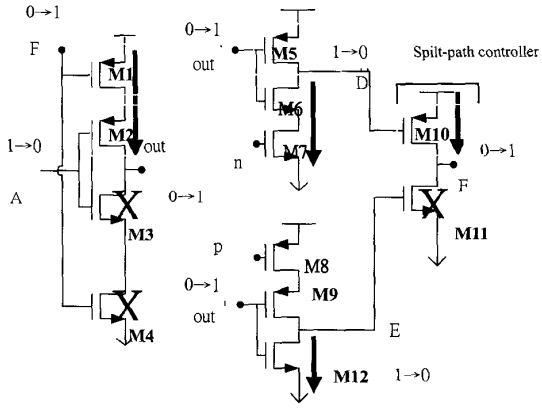


Fig. 6 The out pull-high operation

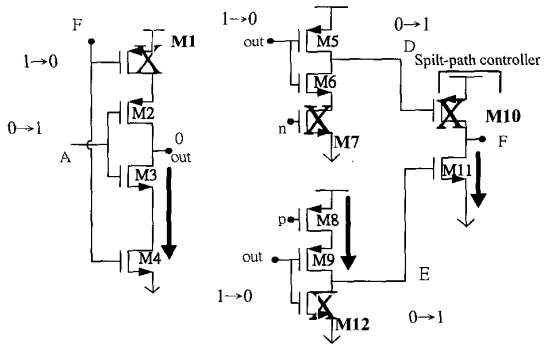


Fig. 7 The out pull-low operation

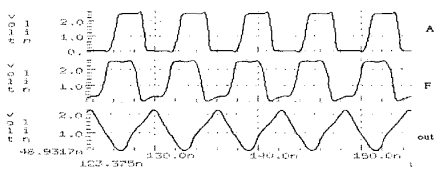
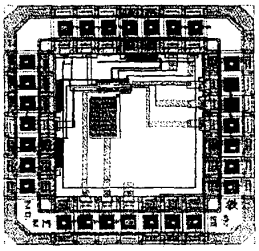


Fig. 8 The waveform of A, F and out



HDPLL

conventional ring VCO			low power VCO		
Vin(V)	Frequency (MHz)	Power (mW)	Vin(V)	Frequency (MHz)	Power (mW)
0 ~0.6	60	1.45	0 ~0.6	48	1.23
0.8	67	1.58	0.8	62	1.44
1.0	95	2.06	1.0	120	2.27
1.2	135	2.76	1.2	197	3.21
1.4	176	3.58	1.4	265	4.11
1.6	207	4.29	1.6	327	4.94
1.8	218	4.65	1.8	366	5.56
2.0	224	4.82	2.0	382	5.91
2.2	227	4.93	2.2	387	6.12
2.4	229	5.01	2.4	392	6.26
2.6	230	5.05	2.6~3.0	404	6.40~6.47
2.8~3.0	231	5.12			

Table 1. The simulation results

	Low-Power VCO	Ring VCO
Frequency range	48~ 404	60 ~ 231
Maximum power dissipation	6.47@404MHz	5.12@243MHz
Minimum power dissipation	1.23@48MHz	1.45@60MHz
Power-frequency ratio (mW/100MHz)	1.47	2.15
Average gain (MHz/V)	148	77

Table 2. The comparison results of the two VCO

VCO output frequency (MHz)	Power consumption (mW)	Locked time (us)	Cycle jitter (ps)	Long-term jitter (ps)
200	4.01	3.1	450	550
240	4.53	2.85	350	415
300	5.29	2.72	125	160
320	5.80	2.65	90	100
400	7.58	2.42	26	70
414	7.65	2.37	21	50

Table 3. The simulation results of HDPLL