A Low-Jitter and Low-Power Phase-Locked Loop Design

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Abstract

This paper describes a design of digital phase-locked loop (DPLL), which has low-power consumption and low jitter feature. Novel voltage controlled oscillator (VCO) and phase frequency detector (PFD) are proposed to reduce the total power consumption and phase error of the DPLL. The proposed VCO has low power consumption, and the PFD is a "three-state" structure with dead zone is 5ps. The power consumption of the proposed DPLL is lower than 6.7mW, and the output-frequency range of the oscillator is from 200MHz to 650MHz. The worst-case cycle jitter is lower than 160ps, and long-term jitter is lower than 220ps. We confirm the results based on 0.5um CMOS technology and 3V supply voltage.

1. INTRODUCTION

Phase-locked loop is a basic component used frequently in many analog and digital systems. Phase-locked loop can be used in clock recovery of communication system and frequency synthesizer of wireless communication system[1][6]. Recently, low power consumption has become the main trade -off in the modern VLSI design, owing to fast development of mobile electronic system[7][8]. Thus, the goal of our paper is to design a low power phase-locked loop.

VCO is an important component of the PLL because the VCO dominates the power consumption of PLL. Therefore, we propose a VCO with low power consumption.

The PFD is also an important component reducing the phase error and locked time of the PLL. In general, "three-state" structured PFD has large dead zone; "four-state" structured PFD has large gain, which makes the phase offset of the charge pump when PLL locks. Consequently, the phase error increases. For these reasons, we propose a "three-state" structured PFD with 5ps dead zone to reduce the phase error of the PLL.

2. DIGITAL PHASE-LOCKED LOOP OVERVIEW

A block diagram of a simple digital phase-locked loop is shown in Fig. 1. At first, the PFD begins to detect the phase error between the reference signal U1 and feedback signal U2. The digital signals of PFD output control the VCO through the charge pump (CP). The loop-filter (LF) can filter the noise and the high-frequency part of output signal of the CP and hold in lock. The frequency divider (FD) is sometimes placed in the feedback loop to make the VCO multiply frequency of the reference signal U1.

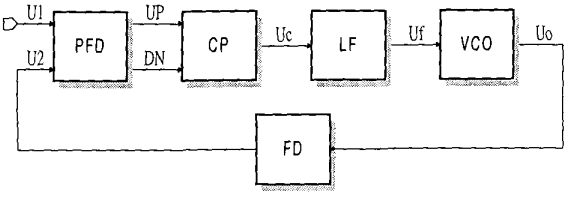

Fig 1 . DPLL function block diagram

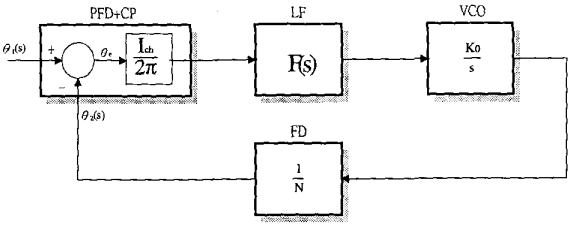

Fig 2. DPLL linear model transfer function

The linear model of this DPLL is shown in Fig. 2[3]. The variables $\theta 1$ and $\theta 2$ are the phase of the reference signal U1 and feedback signal U2. The parameter K0 is the gain of VCO, and N is the divisor of the frequency divider. The close-loop transfer function H(s) is

$$H(s) = \frac{\omega_n^2 + 2\zeta\omega_n s}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

ωn is the nature frequency, and ζ is the damping factor.

3. LOW POWER VCO DESIGN

The programmable delay element is an important component in the low-power VCO design. The VCO dissipates much power when output voltage of delay element varies from (VDD-|Vtp|) to (Vtn+VSS). The VCO has large power dissipation due to the large short circuit current flowing from VDD to VSS. As shown in Fig. 3, if the transition time of the node voltage of N1 or N2 from (VDD-|Vtp|) to (Vtn+VSS) is too long, it will cause large short circuit current of the delay element.

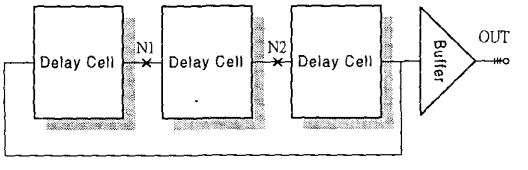

Fig 3. The general VCO Block.

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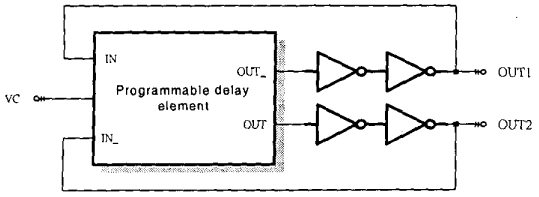

Fig. 4 .The proposed low power VCO.

The block diagram of the proposed VCO shown in Fig. 4 has three low-power features : (1)use only one programmable delay element. (2)no short circuit current. (3)the programmable delay element can shorten the output transition time to reduce the short circuit current of the next stage.

The basic circuit block of the proposed delay element is composed of two C^2MOS inverters with four switches and controlled currents shown in Fig. 5. Two C^2MOS inverters are connected as a regeneration latch to reduce the time cost of output changing from (VDD-|Vtp|) to (Vtn+VSS). Moreover, owing to the feedback control, the circuit has no short circuit from VDD to VSS. In Fig. 5, the switches S2 、S3 are controlled by the input IN+; the switches S1 、S4 are controlled by the input IN-. If the IN+ rises to high and IN- falls to low, the switch S2 is turned on and current source I2 begins to discharge the OUT-; the switch S1 is turned on and current source I1 begins to charge the OUT+. The voltage of the OUT- decreases slowly. The channel CH1 hasn't been turned on until the OUT- decreases lower than (VDD-|Vtp|). Then voltage of OUT+ is charged to VDD quickly. In the same way, the voltage of the OUT+ increases slowly. The channel CH2 hasn't been turned on until OUT- increases higher than (Vtn+VSS). And then the voltage of OUT- is discharged to VSS quickly. The result is shown in Fig. 6. During the transient time, no short circuit current flows from VDD to VSS because only channels CH1 and CH2 are turned on.

In the reverse case, the IN- rises to high and IN+ falls to low. The channel CH3 is turned on and then OUT- is charged to VDD fast; the channel CH4 is turned on and then OUT+ is discharged to VSS quickly. Since only channels CH3 and CH4 are turned on, no current flows from VDD to VSS, either. In Fig. 6, the output of the programmable delay element has very short transition time; therefore it can reduce the short circuit current of the next stage. As a result, the proposed programmable delay element can reduce the power dissipation of the VCO.

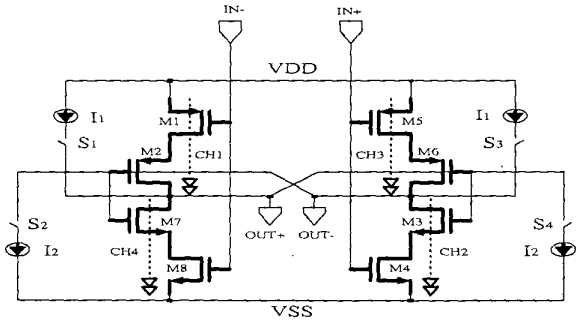

Fig 5. The circuit of the proposed programmable delay element.

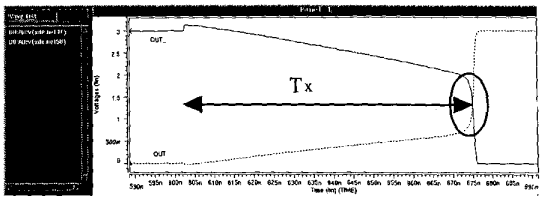

Fig 6. The output waveform of the proposed programmable delay element.

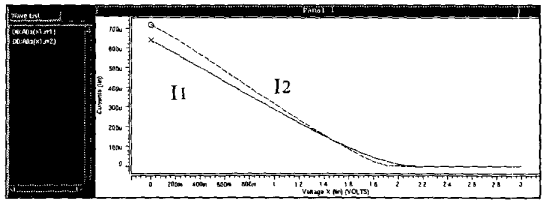

Fig 7 . The controlled currents I1 、I2.

The control current I2 is used to discharge the output nodes of the proposed programmable delay element from VDD to (VDD-|Vtp|), and this time cost is the main delay time Tx. The capacitive load of the output node also controls the delay range of the delay element.

In order to get a better linearity between input voltage and output frequency in VCO, the controlled currents I1 、I2 must have good linearity, as shown in Fig. 7. The controlled voltage range of the proposed element is from 0V to 1.8V.

In general, the C^2MOS inverter has two circuit structures, as shown in Fig. 8. The circuit shown in Fig. 8(a) has the charge sharing problem because the signal IN changes faster than the signal CLK. This makes Q2 or Q3 turned on too quickly. It makes the output OUT has charge sharing with parasitic junction capacitance. Charge sharing makes incorrect charge and discharge and causes the deviation of delay time. In order to reach the high frequency stability and small phase error in the VCO, the circuit shown in Fig. 8(b) is used.

The problem clock feedthrough is a charge injection error on the output nodes, which brings unwanted charge into output nodes. In the Fig. 9, when the current source I2 discharge the node OUT-, the voltage of the output OUT+ reduces a ΔV from zero because the coupling effect of the parasitic capacitance. The clock feedthrough problem causes a variation of delay time, making an unbalance of the duty cycle of the delay element. And then the phase error of VCO will increase. In order to cancel the clock feedthrough problem, we add two current sources I1 to compensate the coupling effect.

The integrated circuit of proposed programmable delay element is shown in Fig. 10.

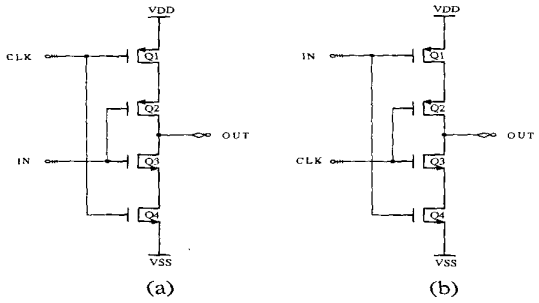

Fig 8. The C^2MOS inverters.

The simulation results of the proposed VCO are shown in Table 1. The highest frequency of the proposed VCO is 650MHz. As the output frequency is lower than the 200MHz, the jitter will increase. Thus the turning range of the proposed VCO is from 200MHz to 650MHz for low jitter application. The total power of the VCO is lower than 4.86mW. This shows the short circuit current has been reduced in the proposed delay element.The design is based upon 0.5 μ m CMOS technology with 3V supply voltage.

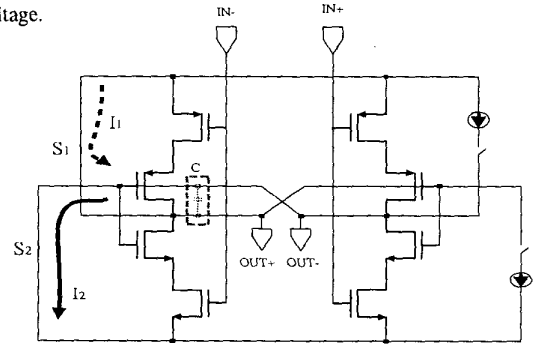

Fig. 9 The clock feedthrough problem.

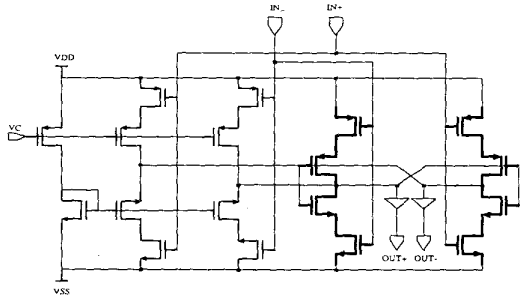

Fig. 10 The schematic of proposed programmable delay element.

Controlled Voltage (V)	Frequency (MHz)	Power (mW)
0.1	662	4.86
0.2	650	4.77
0.4	627	4.55
0.6	590	4.29
0.8	550	3.98
1.0	500	3.60
1.2	437	3.20
1.4	367	2.76
1.6	278	2.20
1.8	174	1.50
2.0	77	1.30

Table 1. The simulation results of the proposed VCO.

4. "THREE-STATE" PFD with 5ps DEAD ZONE DESIGN

$$I_d = I_{ch} \times \frac{\Delta\theta}{2\pi} = \frac{I_{ch}}{2\pi} \times \Delta\theta = K_d \times \Delta\theta$$

The first component of the DPLL is PFD, which controls the locked time and jitter of the DPLL. The output of the PFD depends on both the phase and frequency of its inputs. It compares the leading edges of the reference signal U1 and feedback signal U2. If the phase error is $\Delta\theta$, the output average current of charge pump can be written as
where Kd is the gain of PFD, Ich is the current source of charge pump.

Dead zone is an important parameter of the PFD. And not all PLL using no dead-zone PFD can have the better jitter because the VCO also has the jitter. And the PFD can not detect this random jitter. A good way is to use the PFD with few dead zone. In this way, we can reduce the gain of the PFD of when PLL in locked, and reduce the charge or discharge time of the charge pump.

We propose a "three-state" PFD with dead zone is 5ps shown in Fig. 11[2][4][5]. When frequency of the U1 and U2 are equal, the outputs of PFD have glitches due to the internal race problem of the dynamic logic. We reduce the gain of PFD and place a decreased buffer to reduce the glitches. The output waveform is shown in Fig. 12.

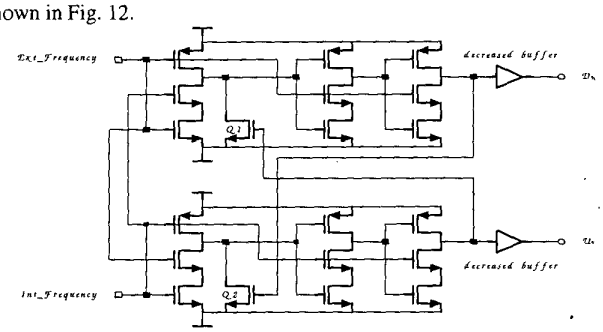

Fig 11. The schematic of proposed phase frequency detector

5. CHIP LAYOUT AND SIMULATION RESULTS

The chip Layout of the proposed low-power PLL is shown in Fig. 12, the total area is 0.837mm^2.The simulation results of the proposed PLL are shown in Table 2 and Table 3. The total power of the proposed PLL is lower than 6.7mW, and cycle jitter is smaller than 160ps. The design is based upon 0.5 μ m CMOS technology with 3V supply voltage.

VCO OUTPUT FREQUENCY	POWER CONSUMPTION	LOCKED TIME	CYCLE JITTER	LONG-TERM JITTER
650MHz	6.7mW	2.7us	23ps	80ps
500MHz	5.8mW	18.8us	10ps	45ps
400MHz	5.2mW	18.8us	30ps	80ps
300MHz	4.6mW	18.6us	100ps	160ps
200MHz	4.1mW	17.1us	160ps	22ps
without noise				

Table 2. The simulation results of the proposed PLL.

TECHNOLOGY	UMC 0.5UM 2P2M CMOS
Supply Voltage	3V
Chip Area	$0.924 \times 0.9 mm^2$
Input Locked Range	50MHz～162.5MHz
Power Consumption	3.6mW～6.7mW
Locked Time	2.7us～18.8us
Long-Term Jitter	45ps～220ps
Cycle Jitter	10ps～160ps
Bandwidth	509.6kHz
Damping Factor	0.16

Table 3 .The specification of the proposed PLL.

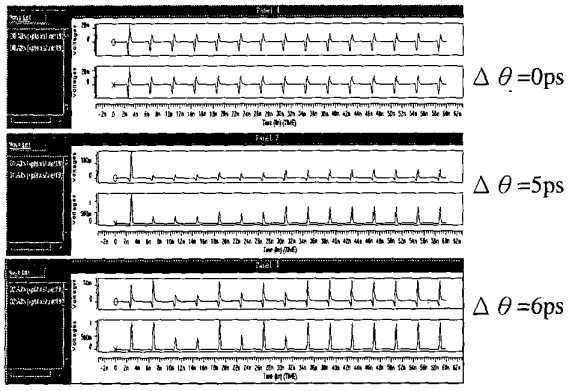

Fig 11. The output waveform of PFD

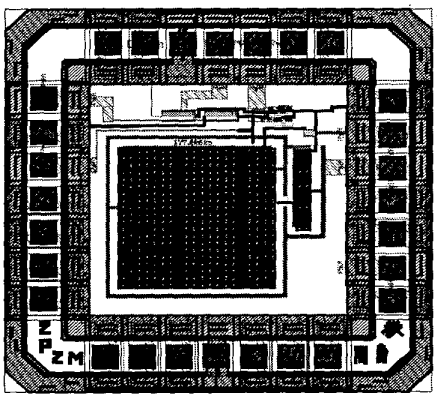

Fig 12. The chip of the proposed PLL

6. CONCLUSION

In this paper, a low power DPLL has been proposed and analyzed. And a low-power programmable delay element is proposed in this design of the PLL. This work proposes novel voltage control oscillator and phase frequency detector to reduce the total power consumption and phase error of the DPLL. The programmable delay element of the proposed VCO has three features: (1)use only one programmable delay element. (2)no short circuit current. (3)the programmable delay element can shorten the output transition time to reduce the short circuit current of the next stage. The power consumption of the PLL is lower than 6.7mW. The worst-case cycle jitter is smaller than 160ps, and long-term jitter is samller than 220ps. The frequency range of VCO is operated from 200MHz to 650MHz. The chip of proposed DPLL is implemented with 0.5um CMOS process technology. The layout area of the chip is $0.837 mm^2$.

7. REFERENCE

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