Accurate Current Mirror with High Output Impedance

Kuo-Hsing Cheng, Chi-Che Chen and Chun-Fu Chung Dept. of Electrical Engineering, Tamkang University, Taipei Hsien, Taiwan, R.O.C

TEL: 886-2-26215656 ext 2731 FAX: 886-2-26221565

E-mail: cheng@ee.tku.edu.tw

ABSTRACT: Current mirror is one of the key elements in analog circuit design. For high performance analog circuit applications, the accuracy and output impedance are the most important parameters to determine the performance of the current mirror. In this paper, a new current mirror is proposed to provide high accuracy and very high output impedance. A novel feedback gain stage is used to increase the output impedance and matching accuracy significantly. Moreover, the proposed new current mirror also has output swing similar as traditional two-stage cascode current mirror.

1. INTRODUCTION

As the current-mode approach used to analog circuit design [1] – [5] is gaining interest due to better performance. Another compelling reason for current-mode circuit is decreasing power supply voltage of digital microelectronics thus it suitable for mixed mode applications. In analog circuit design, the current mirror is widely used in the biasing or the loading elements. It can reduce the current variation due to the power and the temperature variation by using current mirror as the biasing element. Thus the current mirror is the key element in the analog circuit design.

The accuracy and output impedance are the most important parameters to determine the performance of the current mirror. It can find many researches focus on these two points. The cascode current mirror [6] and the RGC current mirror [7] were used to increase output impedance. IAFCCM [8] was proposed to improve the accuracy. Multi-stage cascode current mirror has been used to achieve higher output impedance. It, however, suffers from low output voltage swing. Although the output impedance of RGC current mirror is much higher than that of the two-stage cascode current mirror, but the accuracy of the RGC current mirror is not good enough for high precision application. The IAFCCM has better

accuracy than RGC current mirror, and the output impedance of IAFCCM is equivalent to the RGC current mirror.

In the paper, a new high output impedance current mirror is proposed. The new current mirror is based on the RGC circuit to improve the output impedance and also to improve the accuracy of the current mirror. A novel feedback gain stage is used to increase the output impedance and matching accuracy significantly. Moreover, the proposed new current mirror also has output swing similar as the traditional two-stage cascode current mirror, therefore, the performance of the propose current is better than that of RGC and IAFCCM.

2. DESCRIPTION OF PREVIOUS CIRCUITS AND THE NEW CURRENT MIRROR

2.1 Previous current mirror circuits

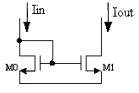


Fig.1 Traditional current mirror

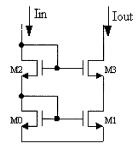


Fig.2 Cascode Current mirror

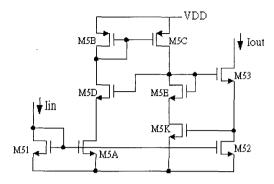


Fig.3 IAFCCM

Figure 1 shows the traditional current mirror. Due to the output impedance of the traditional current mirror is not infinite, the variation of the output node voltage V_{DS1} will influence the output current Iout. It is a drawback in the applications of the analog circuits. As shown in Fig.2, the cascode current mirror was proposed to improve the output impedance, but it has the matching accuracy problem.

The IAFCCM shown in Fig.3 was proposed to increase the output voltage swing, output impedance and matching accuracy [8]. Even though the IAFCCM improves lots of the output voltage swing, but the output impedance is not high enough. Meanwhile, the output current Iout still can be influenced by the output node voltage.

2.2 The proposed new current mirror circuit

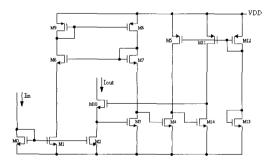


Fig. 4 The proposed current mirror

As mentioned earlier, the key parameters of the current mirror, the matching accuracy and output impedance can be improved by the proposed new current mirror. The schematic of the proposed new current mirror is shown in Fig.4.

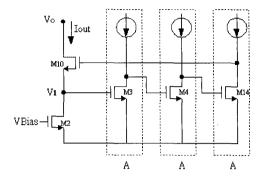


Fig.5 The feedback circuit

The MOS transistors M0, M2 and M10 are used as a two-stage cascode current mirror. The biasing MOS transistors M1, M6, M9, M7 and M8 are used to improve the matching accuracy of the cascode current mirror. Three novel negative feedback gain stages M3, M4 and M14 can increase the output impedance of the current mirror significantly.

Figure 5 is the feedback circuit of the current mirror and "A" represents the voltage gain of each gain stage. The output impedance Rout of the new current mirror can be estimated by following:

$$V_{1} = i \frac{1}{gd2}$$
 [1]

$$i = gm_{10} * (-|A|^{3} - 1) * V_{1} + gd_{10} * (Vo - V_{1})$$
 [2]

$$\Rightarrow i * \left(1 + \frac{gm_{10}}{gd_{2}} |A|^{3} + \frac{gm_{10}}{gd_{2}} + \frac{gd_{10}}{gd_{2}} \right) = gd_{10} * Vo$$

$$\Rightarrow \frac{Vo}{i} = \frac{1 + \frac{gm_{10}}{gd_2} |A|^3 + \frac{gm_{10}}{gd_2} + \frac{gd_{10}}{gd_2}}{gd_{10}}$$

$$\approx \frac{gm_{10}}{gd_{10}} |A|^3 \frac{1}{gd_2}$$
 [3]

$$\Rightarrow Ro = \frac{gm_{10}}{gd_{10}} \frac{1}{gd_2} |A|^3$$
 [4]

As shown in Eq.(4), where
$$A \cong -\frac{gm_i}{gd_i}$$

(i=3,4 and 14, respectively) , the Rout of the proposed current mirror is much larger than that of the IAFCCM which has output impedance

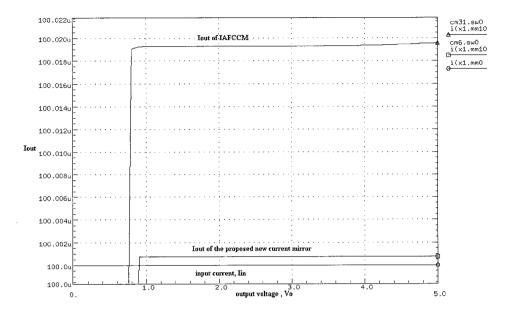


Fig. 6 The I-V curve of the simulation result

$$Rout = gm_{53}gm_{5K} \frac{1}{gd_{52}} \frac{1}{gd_{53}} \left(\frac{1}{gd_{5K}} // \frac{1}{gd_{5C}} \right)$$

As shown in Fig.5, the node voltage V_1 is independent of V_0 and can be proven as following. When V_0 and V_1 are increased which decrease Vds_{14} due to the three gain stages. The voltage Vds_{14} is connected to the gate of M10 as a negative feedback signal. Therefore, V_1 is decreased by the decreased Vds_{14} . Thus, V_1 is locked by the negative feedback loop. In other words, the variation of V_0 cannot result in the variation of V_1 . So we can obtain stable Iout. Meanwhile, the proposed new current mirror has high output impedance.

Another factor of a good current mirror is the matching accuracy between Iin and Iout. In the proposed circuit, the MOS transistors M6, M7, M8 and M9 are used to match the current $I_{\rm M1}$ and $I_{\rm M2}$, and further make $V_{\rm GS3}$ equal to $V_{\rm GS1}$. Because of $V_{\rm GS1}{=}V_{\rm GS0}{=}V_{\rm DS0}$ and $V_{\rm GS3}{=}V_{\rm DS2}$, it is easy to find that $V_{\rm DS2}{=}V_{\rm DS0}$ which results in Iin equal to Iout .

In view the properties and advantages, the proposed current mirror has better current matching accuracy than the IAFCCM, and it will be proven by the HSPICE simulation results.

3. SIMULATION RESULT

The HSPICE simulation results are based upon 0.35um 1P4M CMOS process with 3.3V supply voltage. L=1um for all transistors except M8 and M9 which L=3um. W is 20um for M0 M1 M2 M3 M6 M7 M10 and W is 40um for M8 M9 to ensure Iout=100uA. W is 5um for M4 M14, W is 10um for M5 M11, and W is 1um for M12 M13.

Figure 6 shows the I-V curve simulation results of the proposed new current mirror and IAFCCM. The lowest line is the I-V plot of the input current lin. The top line is the I-V plot of IAFCCM, and it shows that the output impedance is not high enough to avoid the influence of V_{DS}, i.e. Iout will be changed under the variation of the output voltage Vo. The middle line is the I-V plot of proposed circuit, and it demonstrates that the output impedance of the proposed circuit is much higher than IAFCCM. Figure 6 also shows the comparison result of the accuracy. The matching accuracy of the proposed circuit is better than IAFCCM when the input current Iin=100uA. The Table.1 is the comparison result between the proposed circuit and IAFCCM under various input current. The input current is changed from 5uA to 400uA. The proposed circuit has higher matching accuracy, when the input current is lower than 400uA. Due to the MOS transist sizes of the proposed circuit are smaller than IAFCCM, the matching accuracy would worse than IAFCCM when the input current Iin over 400uA. But the output impedance Rout of the proposed circuit is larger than that of the IAFCCM.

Issue	The proposed circuit	IAFCCM
Mirroring error Iin=5uA	0.016%	0.036%
Mirroring error Iin=10uA	0.012%	0.03%
Mirroring error Iin=100uA	0.001%	0.019%
Mirroring error Iin=200uA	0.005%	0.015%
Mirroring error Iin=300uA	0.012%	0.014%
Mirroring error Iin=400uA	0.026%	0.013%
Rout	$\propto \frac{1}{gd} \left(\frac{gm}{gd} \right)^4$	$\propto \frac{1}{gd} \left(\frac{gm}{gd} \right)^2$

Table 1. The proposed CM performance comparison with IAFCCM

4. CONCLUSION

In this paper, a high output impedance and high accuracy current mirror is proposed and analyzed. According to the simulation results, the output impedance and accuracy of the proposed circuit is better than IAFCCM. Obviously, the proposed current mirror is suitable for using in high linearly, high output impedance current output stages, and the operational amplifiers design.

5. REFERENCE

- [1] Song, B.G.; Chang, I.K.; Kwon, O.J.; Park, J.G.; Kwack, K.D. "A simulation-based analog cell synthesis with improved simulation efficiency" TENCON 99. Proceedings of the IEEE Region 10 Conference, Volume: 2, 1999 Page(s): 1018-1021 vol.2
- [2] Handkiewicz, A.; Kropidlowski, M.; Lukowiak, M. "Switched-current technique for video compression and quantization" ASIC/SOC Conference, 1999. Proceedings. Twelfth Annual IEEE International, 1999 Page(s): 299 –303

- [3] Harb, A.; Sawan, M. "New low-power low-voltage high-CMRR CMOS instrumentation amplifier" Circuits and Systems, 1999. ISCAS '99. Proceedings of the 1999 IEEE International Symposium on , Volume: 6, 1999 Page(s): 97-100 vol.6
- [4] Zeki, A.; Kuntman, H. "High-output- impedance CMOS dual-output OTA suitable for wide-range continuous time filtering applications" Electronics Letters, Volume: 35 Issue: 16, 5 Aug. 1999 Page(s): 1295-1296
- Nooshabadi, S.; Visweswaran, G.S.;
 Nagchoudhurhi, D. "Current mode ternary D/A converter" VLSI Design, 1998.
 Proceedings., 1998 Eleventh International Conference on , 1998 Page(s): 244 -248
- [6] P. E. Allen and D. R. Holberg, "CMOS Analog Circuit Design". New York: Holt, Rinehart and Winston, 1987 Page(s):233
- [7] Sackinger, E.; Guggenbuhl, W. "A high-swing, high-impedance MOS cascode circuit" Solid-State Circuits, IEEE Journal of, Volume: 25 Issue: 1, Feb. 1990 Page(s): 289 –298
- [8] Zeki, A.; Kuntman, H. "Accurate and high output impedance current mirror suitable for CMOS current output stages" Electronics Letters, Volume: 33 Issue: 12, 5 June 1997 Page(s): 1042 –1043.