A STUDY ON THE RELATIONSHIP BETWEEN INITIAL NODE-EDGE PAIRS ENTROPY AND MINCUT CIRCUIT PARTITIONING

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Abstract — In this paper, we find the relationship between mincut circuit partitioning and the initial (V, E) pairs distributed condition / entropy on the V-E plain. If a circuit has higher initial potential / entropy, under a nearly max-cut reservation, we have higher probability to aim the mincut. The proposed new method is called Interleaved Cutting — Edge-Node Interleaved Sort for Leaching and Envelop (IC–ENISLE) algorithm. It is not only using node and edge information, but also using max-min dual property. This new method is simple, but works effectively. Hundreds of netlists experiments have ever been processed. It shows we can soon get an intuitive heuristic nearly optimal solution for the mincut and the ratio mincut partitioning at the same time. And the method can display every process step by data compression techniques, is very suitable for IC CAD industrial usage.

Index Term — ENISLE, Max-cut, min-cut partitioning, ratio mincut partitioning, clustering effect, VLSI circuit.

1. INTRODUCTION

Circuit partitioning plays a key role in the design automation of VLSI chips, multichip systems, and system-on-a-chip (SoC). Iterative-improvement two-way min-cut partitioning is an important stage in most circuit placement tools. Recursive two-way partitioning is an efficient and popular approach to obtaining k-way partitions for k > 2 [4], [12]. So many papers are concern here with the two-way mincut partitioning problem. Since two-way mincut partitioning is NP-complete problem [7], a number of approximate schemes have been proposed [6], [8], [10], [11].

Most partitioning techniques for circuit netlists like the Fiduccia–Mattheyses (FM) method, computes the gains of nodes using local netlist information that is only concerned with the immediate improvement in the cutset. This can lead to misleading gain information. This matter let us turn back the origin of the mincut partitioning problems and solving them by global viewpoints.

Let a circuit be represented by a hyper-graph or netlist G = (V, E) where V is the set of nodes that represent components of the circuit and E the set of hyperedges that represent the nets of the circuit. Each hyperedge or net connects two or more nodes together; generally the output of a node is connected to the inputs of several other nodes by a net.
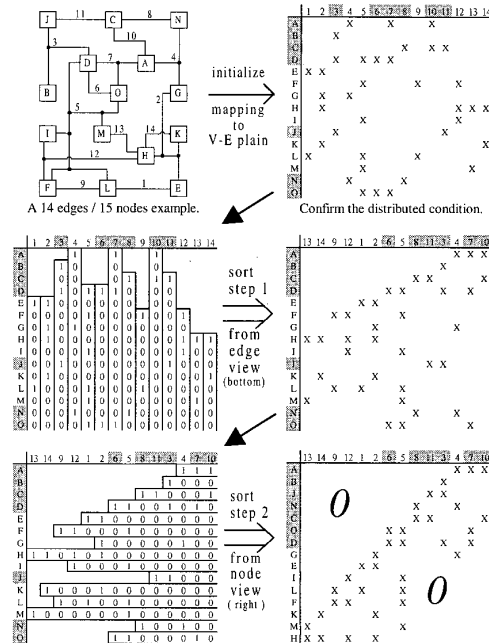
Figure 1. The first two steps of basic ENISLE.

Our goal is partitioning, not only clustering [1]. The first two steps of basic ENISLE for mincut partitioning are shown in Fig. 1 [3]. Notice when (V, E) pairs approach to the uniformly distribution on the V-E plain, and if we can find the min-cut, the "outline areas" of the (V, E) pairs will from the product VE approach to VE/2, like vapor compression behavior.

If the initial "outline areas" of (V, E) pairs occupied on the V-E plain are far less than the VE product, the probability that we can get the min-cut solution is relatively small. This is unlike vapor compression behavior, is like "melting" the material. So first we need "heating" it, adding "entropy" to it. And notice it eases to be randomized.

This paper is organized as follows. In Section 2, show the proposed method and demonstrate by examples. In Section 3, we describe display representation and compression techniques for every process step. Performance Comparisons are given in Section 4. Finally conclude the major findings and outline the future work.

0. **Initialize:** mapping (V, E) pairs to V-E plain, confirm the (V, E) pair distributed condition:
  0A. Randomize the whole node order.
  0B. **Interleave Cutting (IC)-- Separately randomize the two part nodes under a nearly Max-cut reservation.**

1. **Phase One:** basic four steps.

| | E | N | E | N | |
| | (B) | (R) | (T) | (L) | |

E: Edge Radix Sort
N: Node Radix Sort

(B): Bottom-side base
(R): Right-side base
(T): Top-side base
(L): Left-side base

2. **Phase Two Begins:** different additional steps can be choiced.

2A.
| N | E | N | | N | E | N |
| (R) | (T) | (L) | | (R) | (T) | (L) |
○ ○ ○

2B.
| N | E | N | N | E | N | | N | E | N | N | E | N |
| (R) | (T) | (L) | (R) | (B) | (L) | | (R) | (T) | (L) | (R) | (B) | (L) |
○ ○ ○

2C.
| N | E | N | E | E | N | E | N | N | E | N | E | E | N | E | N |
| (R) | (T) | (L) | (B) | (T) | (L) | (B) | (R) | (L) | (B) | (R) | (T) | (B) | (R) | (T) | (L) |

| N | E | N | E | E | N | E | N | N | E | N | E | E | N | E | N |
| (R) | (T) | (L) | (B) | (T) | (L) | (B) | (R) | (L) | (B) | (R) | (T) | (B) | (R) | (T) | (L) |
○ ○ ○

2D.
| E | N | E | N | | E | N | E | N |
| (B) | (R) | (T) | (L) | | (B) | (R) | (T) | (L) |
○ ○ ○

2E. Some other recurring orders.

2F. Some other clustering techniques, like collecting intersection edge vectors.

※ **When** every node sort step completed, record nodes set, and if nodes/cuts no more change, halt the procedures.
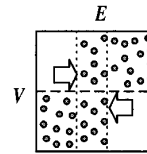
Figure 2. The proposed ENISLE Algorithm family -- include classic ENISLE and IC–ENISLE.

2. THE IC-ENISLE ALGORITHMS

The proposed method called Interleaved Cutting—Edge-Node Interleaved Sort for Leaching and Envelop (IC–ENISLE) algorithms are briefly shown in Fig. 2.

Hypergraphs (circuit) are typical compound tree-based structures. The same level nodes in tree-based structures do not connect each other. In other words, this means the nodes between same levels have no edges. Quickly rough divide the VLSI circuits into two parts, one mainly contains odd-level nodes, another part mainly contains even-level nodes, as shown in Fig. 3. By this interleaved cutting concept, due to the nodes between the same levels have none edges, we get a nearly max-cut partitioning of the VLSI circuit.

Separately randomize the two part nodes as shown in Fig. 4. Notice it only randomize the node number series, do not care the edge number series, because it will be sorted from bottom-side edge base first.

The proposed IC–ENISLE intuitively determine distributed uniformly or not by the diagram clearly, not need additional complex computing about correlation coefficients or co-variances. The Fig. 5 shows the proposed IC–ENISLE algorithm effectively gets the min-cut partitioning and the ratio min-cut partitioning at the same time.

Figure 3. Interleaved cutting the circuit can get an initial nearly max-cut partitioning status.

Seed 1589, (multiplicative congruential) random numbers from 1 to 15:
12 6 5 6 10 14 7 3 9 3 11 6 1 7 9
After Modified...(no repeated number):
12 6 5 8 10 14 7 3 9 13 11 4 1 15 2

Seed 1708, random numbers from 16 to 30:
16 30 16 30 22 19 17 24 26 17 21 24 23 29 17
After Modified...(no repeated number):
16 30 25 27 22 19 17 24 26 20 21 28 23 29 18

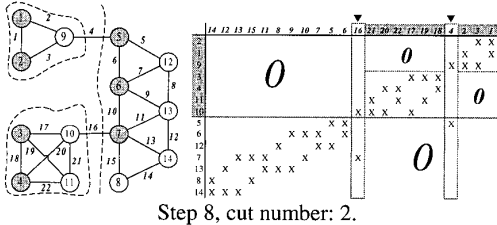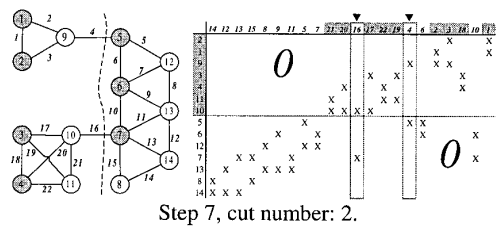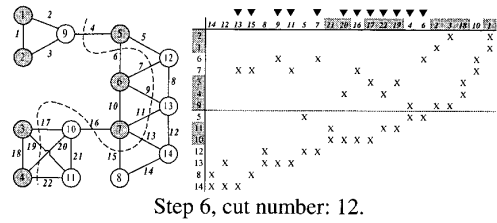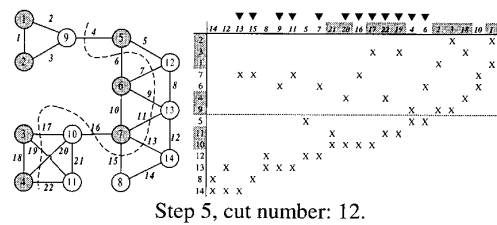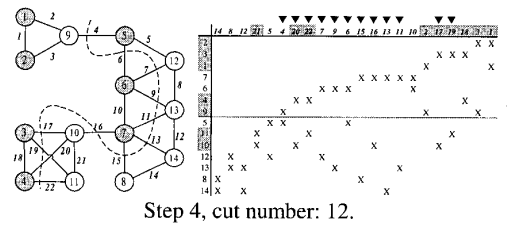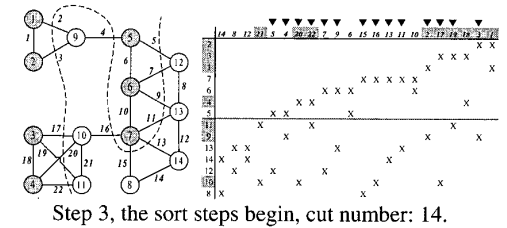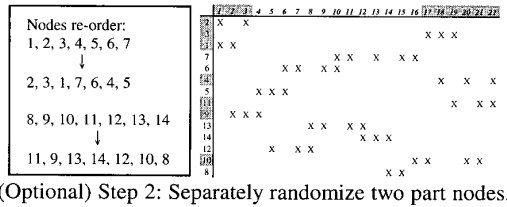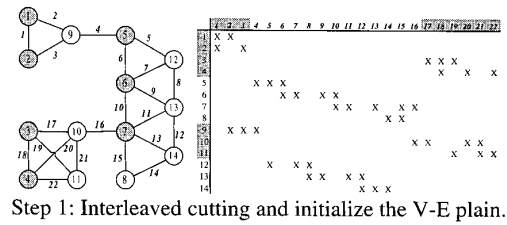**Figure 4.** Separately randomize the two part nodes.

890

Step 1: Interleaved cutting and initialize the V-E plain.

Nodes re-order:
1, 2, 3, 4, 5, 6, 7
↓
2, 3, 1, 7, 6, 4, 5

8, 9, 10, 11, 12, 13, 14
↓
11, 9, 13, 14, 12, 10, 8

(Optional) Step 2: Separately randomize two part nodes.

Step 3, the sort steps begin, cut number: 14.

Step 4, cut number: 12.

Step 5, cut number: 12.

Step 6, cut number: 12.

Step 7, cut number: 2.

Step 8, cut number: 2.

Figure 5. It shows the proposed IC–ENISLE 2A algorithm effectively gets the mincut and ratio mincut partitioning at the same time.

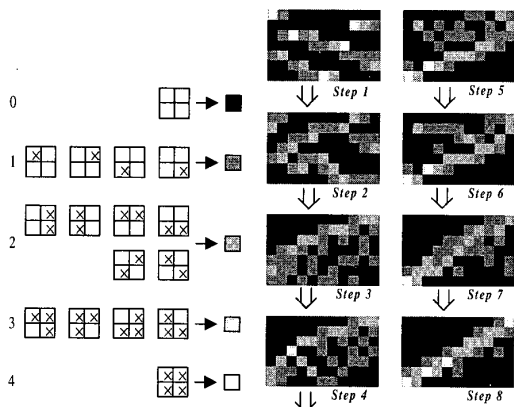**Figure 6**. Data display compression representation of Fig. 5 demonstration.

3. DISPLAY REPRESENTATION AND COMPRESSION
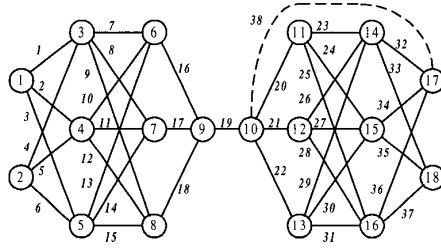
3.1 Display compression by different colors

3.2 Display compression by different light intensity and/or different patterns

One of the useful data compression techniques is shown in Fig. 6. Let L nodes × W edges (V, E) pairs rectangle (if L = W, this is a square) compose a block. The more (V, E) pairs in the block, the higher light intensity. If no (V, E) pair in the block, it is thick darkness. Although display compression lead to miss the exact display positions of (V, E) pairs, just only display it in a block, but we can watch more larger size V-E plain or the whole V-E plain in a monitor screen. And in fact the exact (V, E) pairs positions still be held.
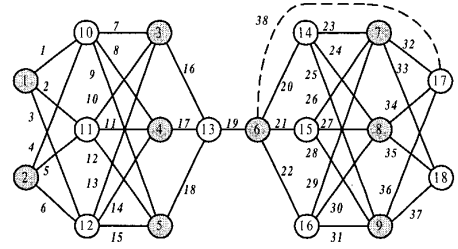
So we can zoom in the V-E plain to watch detail local (V, E) pairs distributed condition, or zoom out to watch global distributed condition.
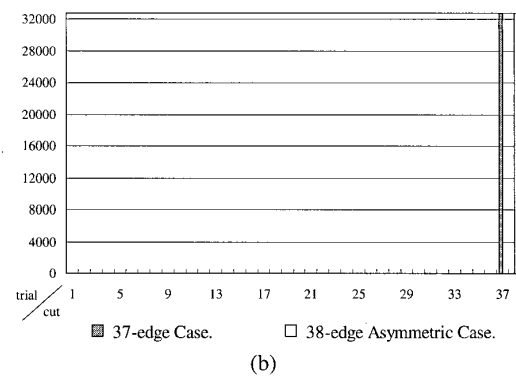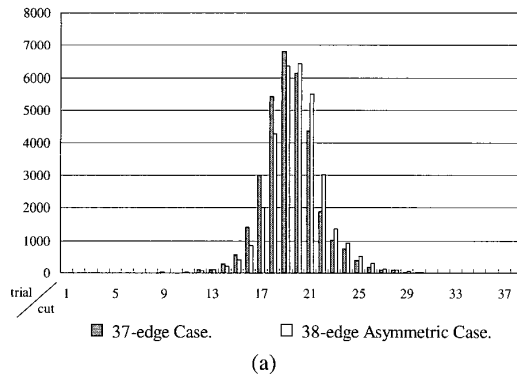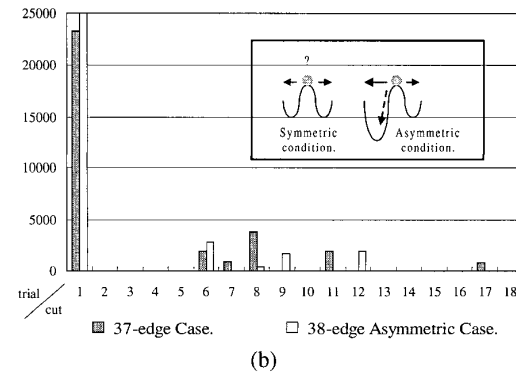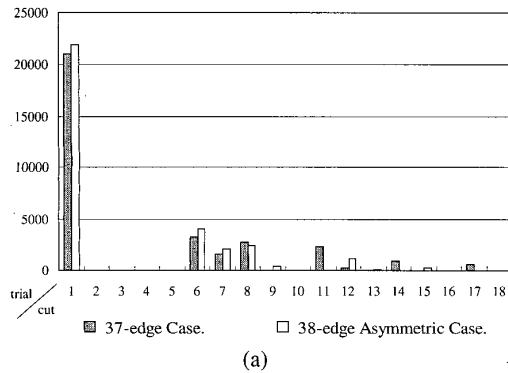
891

Figure 7. Number the circuit from front-end to back-end in sequence.

Figure 8. Number the circuit from front-end to back-end in interleaved levels.

(a)

(b)

Figure 9. The cumulative distribution of initial cut numbers by 32,767 runs with different random order.
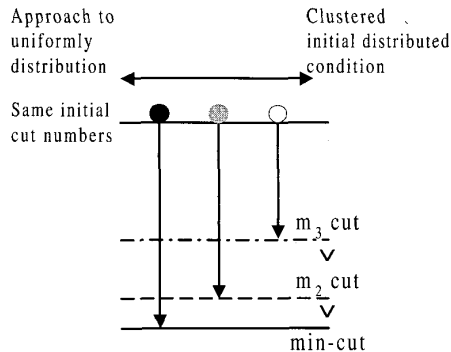(a) Randomize the whole node order. (b) Separately randomize two part nodes under IC.

(a)

(b)

Figure 10. The cumulative distribution of final cut numbers by (a) Classic ENISLE (b) IC–ENISLE.
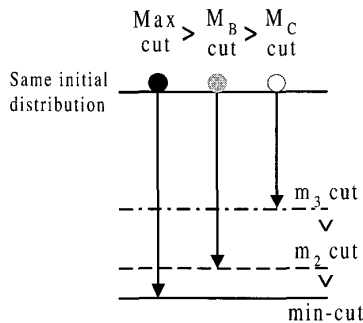
4. COMPARISONS

Fig. 7 and Fig. 8 show a same special circuit and two numbered methods respectively. The difference of the mincut of the circuit (1 cut) and the second mincut (6 cuts) is 5 cuts, is relatively distant. We use the circuit to compare the performance of the classical ENISLE and the new proposed IC–ENISLE algorithm.

The cumulative distribution of initial cut numbers by 32,767 runs with different random order are shown in Fig. 9(a) and 9(b). Fig. 9(a) is a normal distribution. And Fig. 9(b) always keeps the max-cut reservation.

The results are shown in Fig. 10(a) and 10(b). The new proposed IC–ENISLE algorithm is 10.9% (14.1% asymmetric case) better then the classical ENISLE algorithm. The comparisons of the circuits in Fig. 3 and Fig. 5 are further better, but the mincut and other second mincuts are neighbored, so the data information is complex. If the nodes of the two equal-size sets are N, the possible permutations of the whole circuit are (2N)!. And the possible permutations that separately randomize the two part nodes are (N!)×(N!), are the subsets of the possible permutations of the whole circuit.

892

Approach to
uniformly
distribution

Clustered
initial distributed
condition

Same initial
cut numbers

$$m_3 \text{-cut}$$
$$\vee$$
$$m_2 \text{ cut}$$
$$\vee$$
min-cut

Figure 11. The relationship between cut numbers and initial (V, E) pairs distributed condition/entropy.

$$\frac{Max}{cut} > \frac{M_B}{cut} > \frac{M_C}{cut}$$

Same initial
distribution

$$m_3 \text{ cut}$$
$$\vee$$
$$m_2 \text{ cut}$$
$$\vee$$
min-cut

Figure 12. The relationship between max-cut and min-cut: the max-min weak dual property.

5. CONCLUSION

The work finds the relationship between mincut circuit partitioning and the initial (V, E) pairs distributed condition / entropy on the V-E plain:

a. Under a same initial cut number's condition, as shown in Fig. 11, if the circuit has higher initial potential / entropy, we have higher probability to aim the min-cut.

b. Under a same initial distribution, as show in Fig. 12, if the circuit has an initial nearly max-cut reservation, we have higher probability to aim the min-cut.

So the proposed IC–ENISLE force the initial stage not only in higher entropy but also holds a nearly max-cut reservation. Due to VLSI circuits are hypergraphs, we easily get an initial nearly max-cut.

The VLSI circuit mincut is an edge (net) mincut. Vertex (node) min-cut also can be implemented by the proposed method, only add a transformation step:

$$G = (V, E) \rightarrow (E, V) = (V', E') = F$$

The proposed work can get the minimal edge cuts of the network netlists F, and these are the minimal node cuts of the original network G. It may be useful on the network flow problems.

The proposed IC–ENISLE method is not only using node and edge information but also max-min dual property. So its performance is superior to the previous ENISLE. The work shows that we can effectively solve the min-cut and the ratio min-cut partitioning at the same time by global viewpoints.

If we can let (V, E) pairs approach to a uniformly distribution on the V-E plain under an initial nearly maxcut reservation, we can soon get the optimal solution, no more NP-Complete problem.

If we just require certain cut's constraint, our method can provide an intuitive heuristic nearly optimal solution. The method can display every process step by data compression techniques, is very suitable for IC CAD industrial usage.

6. REFERENCES

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893