A NOVEL All DIGITAL PHASE LOCKED LOOP (ADPLL) WITH ULTRA FAST LOCKED TIME AND HIGH OSCILLATION FREQUENCY---

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ABSTRACT

In this paper a new architecture for all digital phase locked loop (ADPLL) is proposed .The new architecture is based on the ADPLL architecture proposed by Motorola in 1995 but modified in some block .A new binary search decision scheme was used to accelerate the frequency acquisition process. It can reduce the chip area and increase the operating frequency. In this design, a 14-bit control word is used to control the digital control oscillator. The new type ADPLL is designed and implement by TSMC's 0-35um IP4M CMOS process for 3.3V applications. The phase lock process takes 20-reference cycle, and the maximum frequency of the proposed ADPLL is about 820MHz.

I INTRODUCTION

The phase locked-loop (PLL) has been widely used for digital system and communication system. It can be used to eliminate the delay between external and internal clock signals caused by the on-chip clock delay. The circuit of PLL needs a reference clock to generates frequency synthesis, duty cycle enhancement, and clock de-skewing .For general application, most of them use half-digital phase locked loop scheme for small chip area. In the architecture of the half-digital phase locked loop, RC low pass filter was used to eliminate high frequency signal and noise. However, the half-digital phase locked loop need longer phase/frequency lock time .An other problem is that the value of R and C manufactured exactly was difficult, in view of the problems of the half-digital phase locked loop, a new architecture of all digital phase locked loop, which was modified from the Motorola's ADPLL architecture in 1995 was proposed .The new architecture avoid using Rand C like conventional half digital phase locked loop and a new binary search decision scheme was used to reduce the phase lock time cycle comparing with Motorola's ADPLL architecture.

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The new architecture also avoids using high frequency for DCO like 74ACT297 and it can operate in high frequency range.

II ARCHITECTURAL OVERVIEW

The ADPLL has four loosely coupled modes of operation for phase/frequency locked procedure: frequency acquisition, phase acquisition, phase maintenance, and frequency maintenance. The phase lock process is separated into frequency acquisition and phase acquisition, which significantly reduced the phase-lock time penalty.

Figure 1 depicts the control unit, 4-state PFD, FG-Register, Add/Sub, Mux, DCO- Register, DCO, and Divider .The operating function of each blocks are shown following. Phase frequency detector (PFD) was used for frequency acquisition and phase acquisition. Different from architecture of Motorola proposed in1995 [1], a new type 4-state PFD was shown in this paper. It uses one hard block to accomplice the behavior of frequency acquisition and phase acquisition. Control unit generates the signals to control all of the sub-block to implement the phase/frequency locked procedure. The FG Register: stores the frequency gain, which will be used during the frequency acquisition mode and phase acquisition mode. The Add/Sub block is arithmetic block. It arithmetically increasing and decreasing the DCO control word to modulate DCO frequency and phase. The function of the Mux in this paper is different from the Mux in Motorola's architecture. It selects the control word from the Anchor register or Add/Sub unit. The stored date of DCO register is to control the frequency and phase of DCO for phase/frequency synthesis. In the initial situation, the DCO register value is set at the half of lock range (i.e.14'hlOOO). The digital control oscillator (DCO) is the key component of the ADPLL system just like the voltage control oscillator (VCO) in half

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digital phase locked loop. The frequency control mechanism of the DCO is through the binary weighted control word from the DCO register. So the magnitude of the DCO control word dictates the frequency requirement of DCO and the control word is held in the DCO register. The function of divider is the same with the divider in the half digital phase locked loop architecture. Phase-locked procedures begin at the frequency acquisition mode. At this mode a modified binary search algorithm sweeps the DCO frequency range

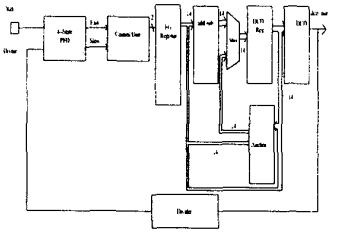


Fig. I the new architecture of ADPLL

(Divided by 16) to match that of the reference clock. The algorithm changes the DCO control word based on the output of the frequency comparator. At the end of frequency acquisition, the ADPLL transfers the DCO control word defining the correct (baseline) frequency to anchor register. When frequency acquisition is complete, the ADPLL enters phase acquisition mode. During phase acquisition, the ADPLL increase or decrease the DCO control word until the phase frequency detector detect a change in the phase polarity of the reference clock relative the internal clock. Phase acquisition is finished when a change in phase polarity occurs. To complete the phase-lock process, the anchor registers transfer its contents to the DCO control register, restoring the DCO control word value representing the baseline frequency. The ADPLL enters please maintenance and frequency maintenance modes. In phase maintenance mode the ADPLL increase or decrease the DCO control word base on the output of the PFD detector. When the phase polarity changes, the contents of the anchor register are transferred to the control register to restore the baseline frequency. In the frequency maintenance mode, the ADPLL will increase or decrease of the anchor register and the baseline frequency is thus changed.

III THE CIRCUIT DESIGN OF ADPLL

In this section, we proposed some novel architecture for PFD and DCO. We know these components arc very impartment for all digital phase locked loop. The design key points for novel PFD arc sensitivity and match delay.

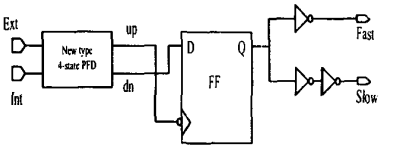
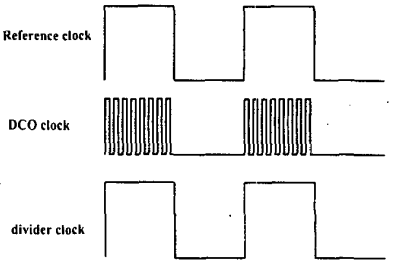
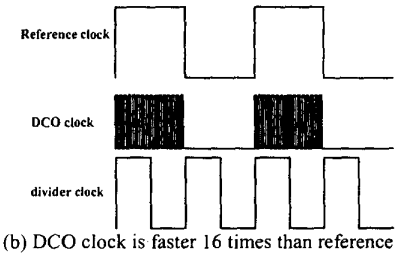


Fig .2 the new type PFD for all digital phase locked loop

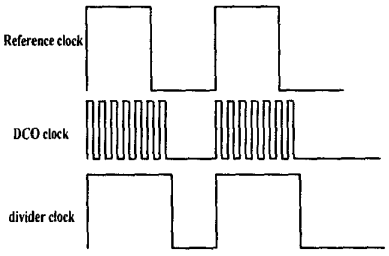
Fig 2 is the architecture of the new type PFD. From the block diagram, we can clearly know that it is consists of two main components. One is a negative edge trigger D-type flip-flop; the other is a new type 4-state phase frequency detector (PFD). A 4-state PFD is a four states finite state machine with two state variables up and dn. In the initial state of phase/frequency comparing is up=1 dn=1 If DCO clock is faster 16 times than reference clock, then the negative edge of divider clock will come before the negative edge of reference clock. For the reason that the output of new type 4-state will be charged to another state up=1 and dn=0.generate third state up=l dn=0. If next situation of the coming of signal is the reference clock negative edge, and the PFD charges to up=0 and dn =0. For the change of up, the D-type flip-flop will be trigged and detected a logical "One" value. Finally the new 4-state PFD can generate a set of output First = 0, Slow = I .For the same reason, we can gat the Fast =l and Slow = 0 result that the reference clock is slower than DCO clock.



(a) DCO clock is just 16 times by reference clock



(b) DCO clock is faster 16 times than reference clock



(c) DCO clock is slower 16 times than reference clock

Fig .3 (a), (b), (c) the wave form of new type PFD

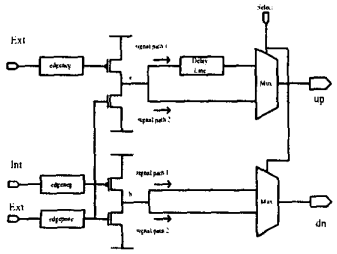


Fig.4 The new type 4-state PFD

Fig .4 shows the circuit of new 4-state PFD. Before the frequency-comparing mode, it is operated in a initial state (i.e. up=dn=l). Reference clock is connected to signal "Ext" and signal "Int" is connected to divider output. For the positive edge of reference clock, NMOS transistor MB and MD will be turned on and then voltage of node "a" and node "b" are discharged to "GND". For the reason, output signal up and dn will be chained to up = I and dn =l as the initial state. Then the new type 4-state PFD will compare which coming of negative edge taster. If the coming of signal "Ext" negative edge is faster than signal "Int", node a will be charged "High" and output "up" will become "Low". For the some reason, we can know the situation of the coming of signal "Int" negative edge is faster than signal "Ext". The other design key issue is delay line match problem. When the ADPLL system operate in frequency acquiescing mode, the control signal "select" is "0" and select the signal control path is " signal path I" as shown Fig .4. The function of the delay line is the some with the delay line in frequency comparator of Motorola's architecture. The matching quality of the delay line reflects the accuracy of the PFD.

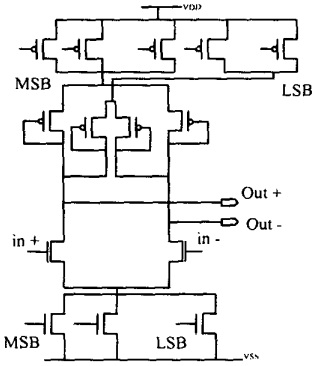


Fig .5 the delay cell of DCO with 10-bit of control

Figure 5 is the delay cell of the digital control oscillator (DCO). Conventional structure of DCO uses inverter as delay cell. Because of using single ending delay cell oscillator cannot generate high frequency with acceptable duty cycle. In our design, differential ending delay cell is used to instead of single ending cell to increase oscillation frequency and duty cycle enhance. A new PMOS switching transistor scheme is used to increase the bit resolution in the differential delay cell. MOS channel width for most significant bits are larger than that of last significant bits. In Fig .6, the circuit of DCO is shown. It also use the bit extension technology that is the same in Motorola's DCO.

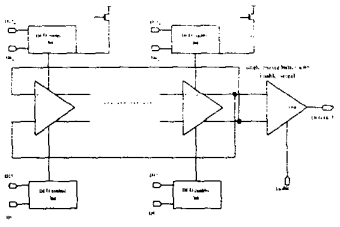


Fig .6 the digital control oscillator block diagram

IV THE ALGORITHM OF NEW FREQUENCY COMPARING

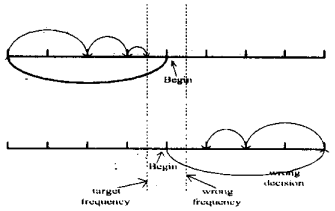


Fig. 7 Example of modified binary search with Motorola's search algorithm

In figure 7, it means a wrong decision caused due to a wrong frequency cannot be recovered. Figure 8 is a frequency binary search-comparing example. The binary search method in Motorola's architecture does not have the "revisit" ability [1]. This phenomenon may occur when the input frequency is at the frequency near the binary checkpoints. A modified binary search algorithm [2] have the "revisit" ability, we still add accelerate searching mechanism for our algorithm. In our algorithm, if there is a change for comparing result such as "fast" change to "slow" or "slow" change to "fast", the value of frequency gain register will divided by 2. The other situation is that the result is success three same out such as success three "fast" or success three "slow", the value of frequency gain register divided by 2 also. It is clear form the decision diagram, shown in Fig .8 in same error decision situation, the proposed new algorithm can faster go to right point and also has "revisit" ability.

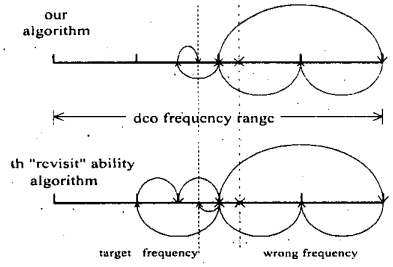


Fig .8 Examples of modified binary search compare with "revisit" ability algorithm

V SIMULATION RESULT

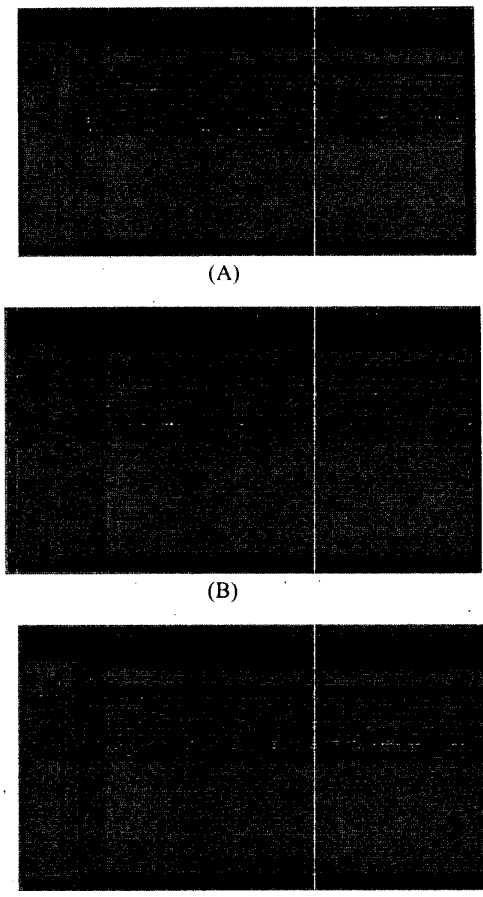


Fig .9 Simulation result (A) frequency comparing mode process (B) phase comparing mode process (C) the final result in phase frequency mode

The lock time of the new type ADPLL is always the half of conventional architecture by using our new type 4-statePFD. The total lock time of the new ADPLL is the cycle infrequency acquisition mode and in phase acquisition. But for conventional architecture is two times cycle in frequency acquisition mode and with cycle in phase acquisition mode. The jitter of the new ADPLL is about 150ps at 730 MHz. The DCO lock range is 680MHz~820MHz.

VI CONCLUSION

In the paper, a new type all digital phase locked loop for high frequency and fast lock process is proposed. A novel4-state PFD is used to reduce the lock cycle time and new differential delay cell is used to improve the lock range enhance the duty cycle match. Base upon the simulation result, the new type ADPLL is designed and implement by TSMC's 0.35um I P4M CMOS process for 3.3V applications.

The simulation tools are used by Verilog-XL for ADPLL model and Hspice for circuits. The phase lock process takes 20 reference cycle, and the locked range frequency of the proposed ADPLL is about 620MHz~820MHz. The jitter of the new ADPLL is about 150ps at 730 MHz.

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