A 10-bit 2.5mW 0.27mm^2 CMOS DAC with Spike-free Switching

Chien-Hung Kuo and Jen-Chieh Tsai

Abstract — *A low-power digital-to-analog converter for portable electronics is introduced. A fully segmented architecture with a spike-free current mirror is presented to improve the INL/DNL and reduce the power consumption of the high-speed current steering DAC. The presented 10-bit DAC have been implemented in 0.18μm 1P6M CMOS standard technology, and its core area is 0.27mm^2. The simulation results show the DNL/INL is ±0.14/0.14 at a conversion rate of 10MHz, and consume 2.5mW of power from a 1.8V supply voltage.*

Index Terms — **digital-to-analog converter, low power, current mirror**

I. Introduction

There is a strong demand to promote the performance of the high-speed digital-to-analog converter (DAC) in many telecommunication systems, such as WLAN, AWG, and HDTV. The full segmented DAC is interested because of their fast operation speed, less consumed area, and high power efficiency. Many efforts have been devoted to improve the resolution and settling time for these current steering DACs. [1]-[2]

The differential switch pair is popular to form the basic current switch in current cell of the segmented DAC. The output voltage of the current cell is hence stabilized while the current branch is cut off. However, a dummy load should be added at the other side of the differential switch to avoid this MOS switch entering cut-off mode. Thus, an additional power would be wasted on this dummy path. Moreover, there are a couple of deglitch circuits are needed to suppressed the spike caused by the abnormal switching on these differential pairs. The extra hardware and their power consumption would be paid.

In this literature, a new high-accuracy current cell with spike-free switching for the full segmented current steering DAC is proposed. The output voltage of the current cell can be kept on a fixed voltage level with no other output path is needed while the current cell is turned off. The power dissipated on the dummy load in the conventional DAC can thus be excluded. Since no deliberated deglitch circuits in the proposed current steering circuit are required, less hardware and power would be achieved for a 10-bit full segmented DAC.

Section II describes the fundamentals for the architecture of the presented DAC. Section III discusses the proposed current cell and simulation results of the presented DAC. Finally, a conclusion is given in section IV.

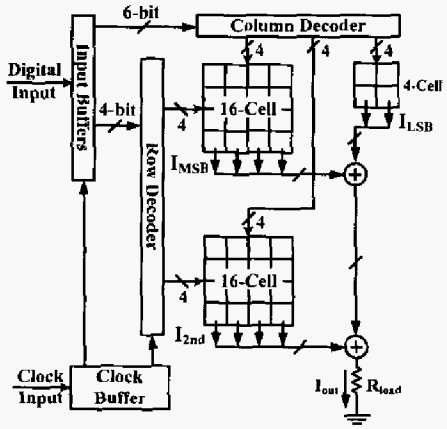

Fig. 1. Block diagram of the DAC

II. Architecture

The block diagram of the presented DAC based on the full segmented architecture is shown in Fig 1. In order to reduce the number of current cells and relax the complexity of the row and column decoder, the three-stage current cell matrix architecture is applied. It is composed of the 4 MSB (B9-B6) bits, the succeeding 4 bits (B5-B2), and the last 2 LSB (B1-B0) bits current cell matrices. In this architecture, only 15+15+3 current cells are needed, the hardware can be reduced considerably compared to 1,024 current cells originally for a 10-bit resolution of the DAC. Three different current levels, I_{MSB}, I_{2nd}, and I_{LSB}, are designed for two 16-cell matrices and one 4-cell matrix, respectively, to perform the presented DAC. And the resulting output current I_{out} can be expressed as follows.

$$I_{out} = I_{MSB}(2^3 b_9 + 2^2 b_8 + 2^1 b_7 + 2^0 b_6) + I_{2nd}(2^3 b_5 + 2^2 b_4 + 2^1 b_3 + 2^0 b_2) + I_{LSB}(2^1 b_1 + 2^0 b_0) \quad (1)$$

[1] This research was supported in part by a grant of making chips from National Chip Implementation Center (CIC)

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where $I_{MSB} = 16 \times I_{2nd}$, $I_{2nd} = 16 \times I_{LSB}$, and b_i, i=0, 1, 2, ..., 9 denotes the digital input bits. Thus, the output voltage V_{out} can be derived as

$$V_{out} = I_{out} \times R_{load} \quad (2)$$

where the resistance R_{load} is the output load.

The current cell matrix with the differential switch pair embedded in the DAC can be shown in Fig. 2. When parts of the switches in solid lines are turned on, the related cell currents will flow into the load to derive the output voltage. Meanwhile, the switches in gray lines will be turned on while the corresponding switches connected to the same current source are off. The voltage fluctuation at the output of each current source can thus be released due to this differential switch pair. However, the power dissipated on this dummy load will be wasted, and then the total power consumption on the whole current cell matrices may be doubled. Furthermore, to smooth the peaking at the output of each current source while the differential switch pair is switching, an additional deglitch circuit must be added. However, the physical sizing for these deglitch circuits might be still corrupted due to the process variation. [3]-[5]

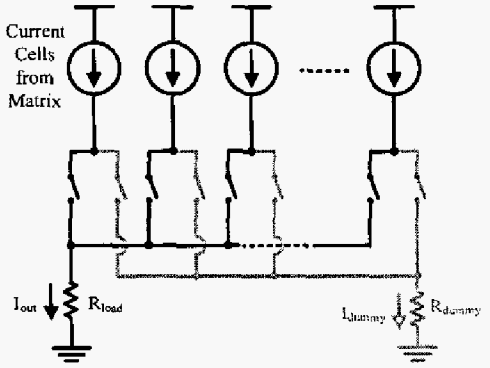


Fig. 2. The current cell matrix

To avoid the voltage fluctuation at the output of current source and the unnecessary power dissipation on the dummy load, a new current mirror with a stable output voltage for the current cell switching is proposed. These new spike-free current cells are applied to the current cell matrices embedded in the presented DAC to save the power and the consumed area.

III. Circuit Implementation

A. The Proposed Current Source for Switching

The conventional current mirror with a differential switch pair can be implemented as shown in Fig. 3. The gain-boosting technique, which is formed by the transistors M6-M7, is applied to the cascode current mirror, M9 and M10, to increase the current accuracy and output impedance of the current source. The differential switch pair (S1 and S2), which is made by a pair of PMOS, is turned on alternatively to stream a steady current from the current source to the output load 1 or dummy load.

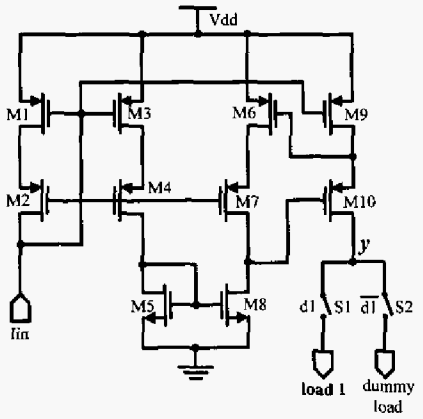


Fig. 3. The conventional current mirror

When the digital input d1 is low, the switch S1 is turned on and the switch S2 is turned off. The current will flow into the output load 1. When the digital input d1 is high, the switch S1 is turned off, the voltage at the output terminal *y* of the current source tends to be approaching the rail level due to its ceasing stream of the current. Therefore, in the meantime, the differential switch S2 must be turned on by providing the other current path to exclude the turn-on time of the current source required. Furthermore, to avoid the spike occur at the outputs of the current sources, a great amount of deglitch circuits must be paid to adjust the switching time between the differential switch pair properly.

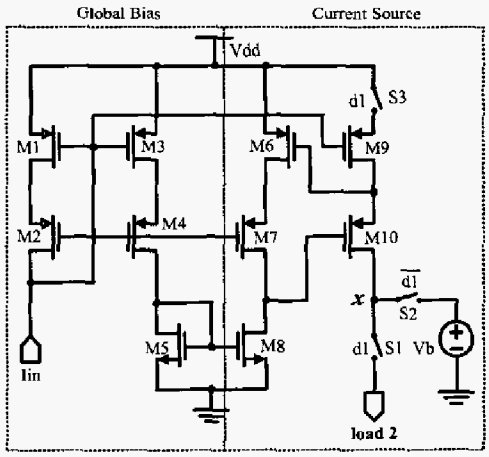


Fig. 4. The proposed spike-free current mirror

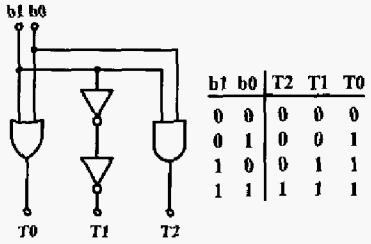
To save the power consumed on the dummy load and reserve the advantage of the unnecessary turn-on time, a new current mirror with spike-free switching is proposed in Fig. 4. Since the voltage at node *x* tends toward the rail

voltage while the current branch is off, the operation speed and the accuracy of the current source would be affected while it should be turned on next time. Therefore, a reference voltage is provided to stabilize the voltage fluctuation of the node x while the switch S1 is off. That is, when d1 is low, the switch S2 will be turned on and the reference voltage Vb will keep the voltage of the node x on a fixed voltage level.

Furthermore, to avoid extra power dissipated on this current branch while switch S2 is turned on, the switch S3 will be turned off to break this current branch at the same time. It should be noted that the current flowed on the reference voltage are designed small enough to limit the power consumed on this reference branch [6]-[8]. Since half the differential switch pair and the deglitched logic circuit are no more needed, the power-hungry dummy load in the DAC can be discarded.

B. Decoder Units

The row and column decoders are made up by a series of 2-bit thermometer code decoders, one of which is shown in Fig. 5, to perform the selection of current cells.



b1	b0	T2	T1	T0
0	0	0	0	0
0	1	0	0	1
1	0	0	1	1
1	1	1	1	1

Fig. 5. The binary-to-thermometer decoder

C. The Proposed Current Cell

Fig. 6 shows the circuit of one unit current cell. It includes a current source and a digital control unit. The current source is the one developed as the aforementioned current mirror. The switch S2 is formed by a PMOS to match the switching characteristics of the switch S1. Two diode connected MOS with low output impedance are implemented to be a reference voltage source. It should be mentioned that the current streaming on this reference branch is designed very small to save the power consumed on it.

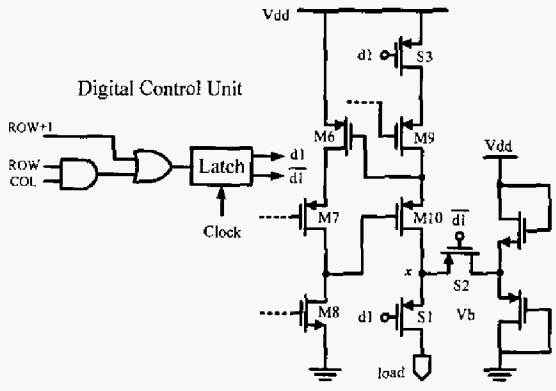


Fig. 6. Current Cell Unit

Whether the current branch is conducted or not depends on its control code derived from the decoder. Since the control code in the high significant bit of the row code basically have to activate the low significant bit of the column one, the row selection code will be dominated by the next row, as shown in the digital control unit of Fig. 6. A succeeding latch is buffered to synchronize the transmission delay caused by the decoders and selection logics. This latch also generates a complementary bit of the selection code for switching the connection of the current source.

IV. Simulation Results

Two proposed current cells with a successive switching digital signal have been simulated in HSPICE to compare to the conventional current ones of Fig. 3. The simulation results are shown in Fig. 7, it can be seen that when digital control d1 is high, the current branch is swapped in the differential switch pair, and the voltage at the node y will exhibit a deviation of 0.5V. In the other hand, the voltage at the node x of the proposed current mirror will almost stay the designed voltage level with reduced deviation during switching. The operation speed of this basic current cell would be maintained because no recovery time is required at the output terminal of the current source. However, the power consumption of each cell can be reduced since the dummy load is discarded. Furthermore, it can also be seen

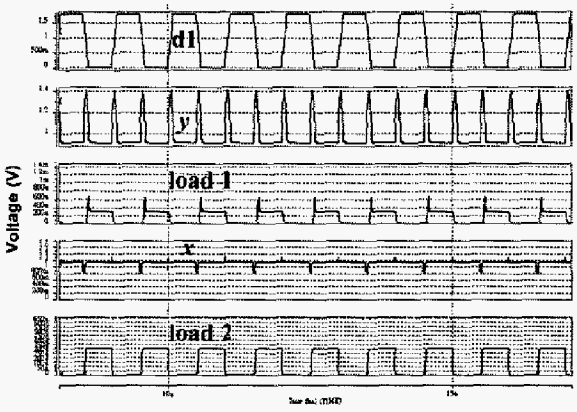


Fig. 7. The simulation results of the current mirrors in Fig. 3 & Fig. 4.

that the voltage at the output load 1 of the conventional current mirror is prone to spiking due to the capacitance effect during switching. And the corresponding voltage at the output load 2 in the proposed circuit behaves a better

transition response because the output voltage of the current source is clamped.

The DAC is simulated with different levels of input applied and the 1,024 output points are taken at a 10M Sample/s from a 1.8V of supply voltage. The differential non-linearity (DNL) and integral non-linearity (INL) of the presented DAC is ±0.14 and ±0.14, respectively.

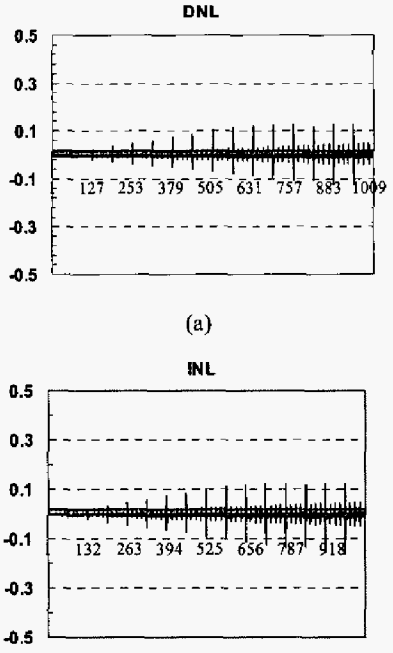


Fig. 8. (a) DNL and (b) INL of the presented DAC

The layout of the presented 10-bit full segmented DAC is shown in Fig. 9. The chip has been implemented in TSMC 0.18um 1P6M CMOS standard process. Three segmented arrays, which occupy the most area in the DAC, are the 16-cell matrix with unit current of I_{MSB}, the 16-cell matrix with unit current of I_{2nd}, and the 4-cell matrix with unit current of I_{LSB}, respectively. The core area without PADs is 0.27mm^2. The performances of the presented DAC are summarized in Table I.

V. Conclusion

In this paper, a new 10-bit 2.5mW DAC with improved current mirror is presented. The proposed current mirror with the stabilized output voltage can be adapted to a high speed switching. The power dissipated on the dummy load of the presented DAC will be excluded. The simulation results show the INL and DNL are within ±0.14/0.14, respectively. The power consumption is 2.5mW at 10MHz of conversion rate from a 1.8V supply voltage.

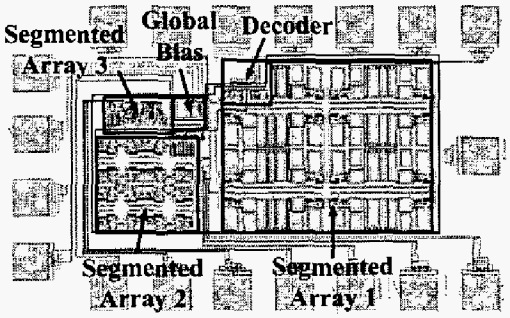


Fig. 9. The layout of the 10-bit DAC

TABLE I
PERFORMANCE SUMMARY OF THE PRESENTED DAC

TECHNOLOGY	0.18μM 1P6M CMOS
Supply Voltage	1.8V
Update Rate	10MHz
Power Consumption	2.5mW
DNL/INL	±0.14/±0.14
Chip Area without PADs	0.27mm^2

Acknowledgment

The authors would like to thank the reviewers for their comments to improve this paper. This research was supported in part by a grant of making chips from National Chip Implementation Center (CIC).

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