A FREQUENCY SYNTHESIZER USING TWO DIFFERENT DELAY FEEDBACKS

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Abstract— **A phase-locked loop (PLL) with two different delay feedback paths is presented. It provides a new approach to minimize the dead zone, jitter accumulation, long settling time and nonidealities on PFD/CP. This PLL utilizes a tunable delay cell to reduce the ripple on the VCO control line and hence the jitter penalty. In addition, a fully differential delay cell for voltage-controlled oscillator (VCO) is introduced to perform a wide locking range and low-jitter performance. The proposed PLL was implemented in 0.35-μm 2P4M CMOS standard technology with the core area of 0.1 mm^2. It can be operated from 250MHz to 1.29GHz and consume 38.2mW of power at 1GHz under a 3.3-V supply voltage.**

I. INTRODUCTION

Phase-locked-loops (PLLs) are widely used in wireless data telecommunications, such as wireless local area networks (WLANs), mobile and satellite communications. In these applications, the PLLs are usually used as a clock synthesis block to generate a high-speed internal clock from an external fixed oscillation source.

There is a tight tradeoff between the settling time and the amplitude of the ripple on the VCO control line in the design of phase-locked loops [1]. This tradeoff for phase-locked RF synthesizers limits the performance in terms of the channel switching speed and the magnitude of the reference sidebands that appear at the output.

This paper presents a double PFDs PLL approach with a tunable delay unit to produce a small ripple on the VCO control line as well as a low jitter performance metric. Besides, the proposed architecture also provide another benefit that less settling time is required compared to the architecture with only one PFD.

Section II develops the fundamental principle for the architecture of the proposed frequency synthesizer. The circuit design and simulation results of the presented frequency synthesizer are shown in Section III and Section IV, respectively. Finally, a conclusion is given in Section V.

II. ARCHITECTURE

There are three main reasons would corrupt the whole PLL performance. First, the large dead zone induced by the PFD, it causes the phase error accumulation at the VCO output. Second, the jitter evoked by the inevitable 1/*f* and white noise of the circuits, it forces VCO to contribute phase noise toward the output. Third, the clock feedthrough and charge injection motivated by CP switches, it results in the abrupt vibrations on the VCO control line and their corresponding clock jitter even when the loop is locked.

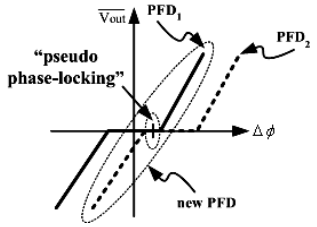

Figure 1. Two PFDs with separate dead zones.

To remedy these imperfections in the circuits, the dead zone of PFD should be effectively regulated and suppressed [2]. Toward this end, two PFD have the same dead zones but unequal phase delay are considered, which are depicted by real and dashed lines, respectively, as shown in Fig. 1. If a new transfer curve could be consist of the right hand curve of PFD_1 and the left hand curve of PFD_2, as illustrated in the ellipse, the shrunk PFD dead zone will be gained. It should be noted that an extra phase offset will be introduced when the PLL is settled, but it would not affect the accuracy of the phase locking process. It is hence referenced as "pseudo phase-locking" to distinguish the conventional scheme. In addition, a fully differential delay cell is used to realize low-noise requirement of the proposed VCO.

The conventional architecture of PLL is shown in Fig. 2(a), where a charge pump and a phase-frequency detector drive a VCO. To reduce the glitch caused by charge pump, a capacitor C_2 is provided to smooth the voltage spurs at every phase comparison instant [1], [3]. However, the voltage jumps can be diminished efficiently by a relative large capacitor C_2 that would consume a considerable chip area and long settling time. In other words, the current of the charge pump should be designed carefully. A large injecting current generated from the nonidealities of PFD/CP would cause a violent voltage ripple on the VCO control line, Vcont. It subsequently results in the VCO output phase error and even causes the system unstable. On the other hand, the small steering current from the CP would result in smaller voltage ripple but longer settling-time. The trade-off between ripple on the VCO control voltage and settling-time should be deliberated upon.

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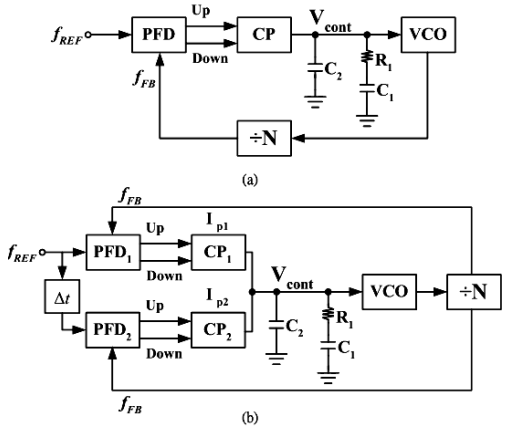


Figure 2. (a) Conventional PLL architecture. (b) The proposed PLL architecture with double PFDs scheme.

The proposed synthesizer is composed of two PFDs, two CPs, a second-order loop filter, a VCO, and a high-speed true single phase clocking (TSPC) D flip-flop divider, as shown in Fig. 2(b). There are two similar PFD paths except the lower one introduces an extra delay time Δt, which is much smaller than the loop time constant. Next, the upper charge pump, CP_1, drives the loop filter first, and after a delay time Δt the lower charge pump, CP_2, stimulates the loop filter again. The total current flowing through loop filter is thus equal to

$$I_p = \pm I_{p1} \pm I_{p2} e^{-s\Delta t} \approx \pm I_{p1} \pm I_{p2}(1 - s\Delta t) \quad (1)$$

where I_{p1} and I_{p2} denote the charge pump currents in upper and lower paths, respectively. The positive and negative signs in (1) indicate the charging and discharging operations, respectively.

As shown in Fig. 3(a), the reference signal and feedback signals are denoted as R_i (i =1, 2) and F, respectively. The symbols U_i and D_i (i =1, 2) represent the "Up" and "Down" signals which are used to control the charge pump to charge or discharge the loop filter. The operations of the proposed architecture are based on the rising edge of signals as below:

- Since there is an additional delay in PFD_2, the reference signal R_2 will lag behind the other signal R_1 by ΔT.
- When the signal F lags behind both R_1 and R_2, two overlapped pulses in U_1 and U_2 are generated by two PFDs, as shown in Fig. 3(b). Hence, more charge pump current is injected into the control line to speed up the charging time.
- Similarly, when signal F leads both R_1 and R_2, two pulses will be presented in D_1 and D_2, as shown in Fig. 3(c). Thus more pump current will flow out of the control line to shorten the discharging time.
- When the signal F falls into the phase slot between R_1 and R_2, two pulses in U_1 and D_2 are produced with the width that is equal to the phase difference between signal F and one of the reference inputs R_1 and R_2, respectively, as shown in Fig. 3(d).

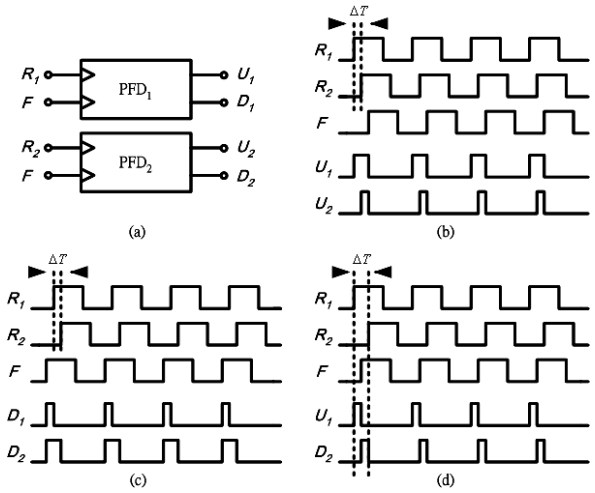


Figure 3. The operations of the proposed PLL architecture. (a) Signal definitions in two PFDs. (b) F lagging R_1 and R_2. (c) F leading R_1 and R_2. (d) F falling into the space between R_1 and R_2.

The amount of the injected charge on the VCO control line is determined by the charge sum of the positive charge and the negative charge. When the system is settling down, the feedback signal will be located between two reference inputs. Assume the dead zones in two PFDs are $\Delta\phi_{D1}$ and $\Delta\phi_{D2}$, respectively. The tuning range of the delay time Δt should follow the relationship:

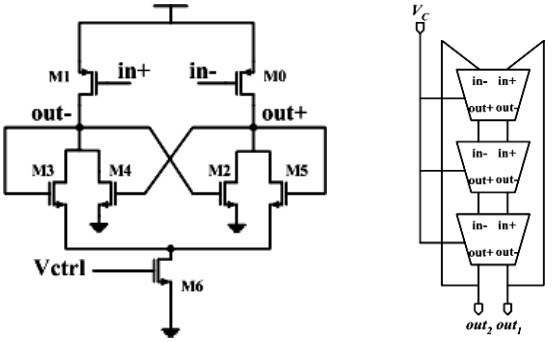
$$0 < \omega\Delta t \le \frac{1}{2}(\Delta\phi_{D1} + \Delta\phi_{D2}) \quad (2)$$

where ω represents the radian frequency of the reference input.

III. Circuit Implementation

A. VCO

The fully differential delay cell and the synthesized ring oscillator are shown in Fig. 4. The differential delay cell structure is adopted to provide the wide locked range and improve the noise immunity. It consists of one PMOS input differential pair, M0 and M1, two cross-coupled feedbacks, M2 and M4, two diode-connected transistors, M3 and M5, and a current source [4]. In this delay cell, the PMOS input differential pair is applied since its less 1/f noise than NMOS counterpart. The sources of the transistors M2 and M4 are directly connected to ground to relax the current limitation and maximize the output swing [4]. The current source of the delay cell can be adjusted by the external gate voltage, Vctrl, of M6 to trimming the transition time. It will subsequently vary the output oscillating frequency of the ring oscillator. To compromise power-linearity tradeoff, the ring oscillator is constructed by three differential delay cells.



(a) (b)

Figure 4. The schematics of (a) the delay cell and (b) the ring oscillator.

B. PFD

The dead zone of the PFD is an important feature that affects the PLL performances essentially. A PFD with large dead zone would cause the PLL output jittered and the locking time consumed. To obtain performance output, the zero dead zone PFD should be well-designed at the cost of complex circuitry and expensive charge [2]. In other words, to minimize the effect of the finite dead zone, the gain of the PFD must be reduced when PLL is locked, and hence a short charging and/or discharging time of the charge pump can be resulted.

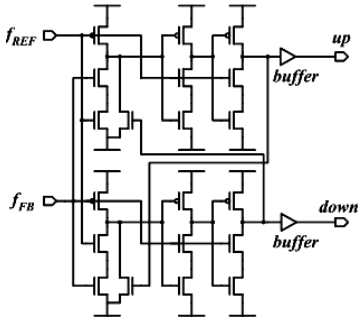
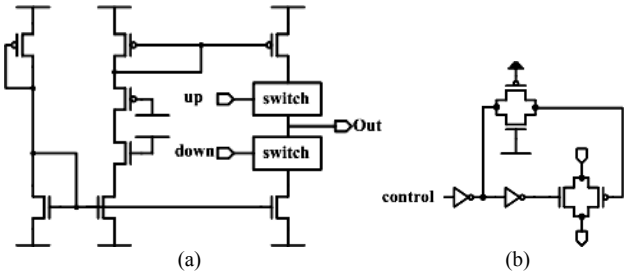


Figure 5. The schematic of three-state PFD with delay buffers.

In this design, a "three-state" PFD is preferred for low power dissipation and less phase error in the PLL, as shown in Fig. 5 [5]-[7]. Since the internal race of the dynamic logics would create glitches on the output even the phases of f_{REF} and f_{FB} are equal, i.e. when PLL is locked, a moderate PFD gain is designed and two additional buffers are inserted to discard the spurs.

C. Charge Pump

For the less impact on output voltage, the current mode charge pump is used, as shown in Fig. 6(a). It consists of a current mirror and two pumped switches. Since the charge injection induced by the parasitic capacitances of the switches in charge pump would impact on the accuracy of the VCO control line, a transmission gate with balance-controlled paths is used to mitigate this issue [8], as shown in Fig. 6(b). An additional transmission gate, which is always on, is inserted to meet the same arrival time on the complementary controls of the switch. Note that there is a second-order low-pass filter is followed to remove out the high frequency noise, as shown in Fig. 2(b).



(a) (b)

Figure 6. (a) Charge pump circuit (b) Switch.

D. Divider

Frequency divider (FD) is used in the PLL feedback path to divide the output frequency for comparing the reference phase of the synthesizer. A high-speed divided-2 divider based on the true single-phase clocking (TSPC) topology [9] is shown in Fig. 7.

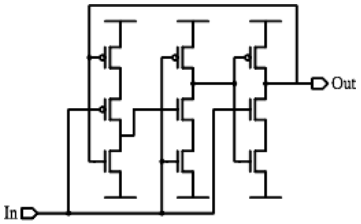


Figure 7. The schematic of the TSPC divider

IV. Simulation Results

To estimate the effect of tunable delay on the synthesizer performance, the behavior simulations of the Fig. 2(b) in different delay quantities are made by MATLAB. Suppose both the PFD dead zones are 20ps for simplicity,

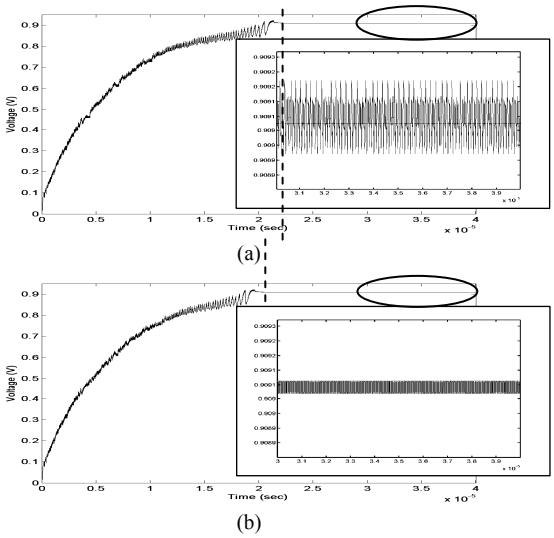
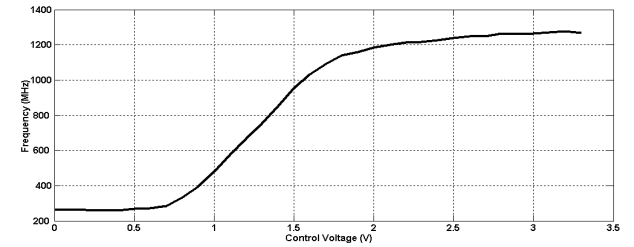


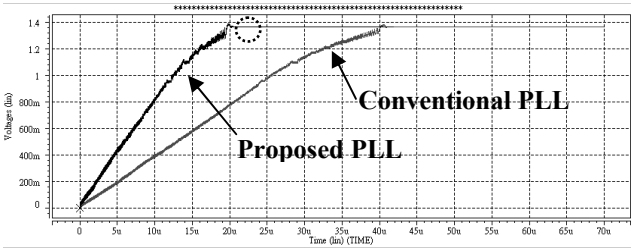
Figure 8. Simulation results of the proposed PLL in Fig. 1(b) when (a) Δt = 90ps (b) Δt = 30ps.

and K_{vco}=1.04 GHz/V, the bandwidth of loop filter is 1MHz. When the delay time of 90ps is set, the voltage ripple on the VCO control line is 0.2mVp-p, as shown in Fig. 8(a). When the delay time is down to 30ps, the voltage ripple on the VCO control line will be suppressed smaller than 0.1mVp-p, as shown in Fig. 8(b). It shows that the ripple swing on the VCO control line can be suppressed by means of less delay time Δt is given.

From the HSPICE simulation results, the proposed PLL can be operated from 250MHz to 1.29GHz, as shown in Fig. 9(a). The power consumptions of the VCO under different control voltages from 0V to 3.3V are measured within the range of 16.1 to 32.3mW. The entire power dissipation of the presented PLL at 1.0 GHz is 38.2mW under 3.3V supply voltage. The cycle to cycle jitter and long term jitter are 7.2ps and 16.6ps, respectively. This PLL was fabricated in TSMC 0.35μm 2P4M CMOS standard process. Its layout photo is shown in Fig. 10. The core area without PADs is 0.28×0.38 mm^2. The performances of the proposed PLL are summarized in Table I. Simulation results show that the double PFDs scheme exhibits shorter settling time, 22μs, than one PFD does, as shown in Fig. 9(b).



(a)



(b)

Figure 9. (a) Operating frequency versus control voltage for the ring oscillator (b) Transient responses of the PLLs.

V. CONCLUSION

In this paper, the proposed PLL that reduces the ripple on the control line as well as jitter is presented. A fully differential delay cell for the VCO is introduced to achieve wide locking range and low-jitter performance. Two PFDs are combined to provide a less dead zone with a new phase-detecting approach and a less settling time. A tunable delay element is used to suppress the ripple on the VCO control line, and hence a more accurate output clock can be resulted. The presented PLL can be operated from 250MHz to 1.29GHz. It consumes is 38.2mW of power at 1.0 GHz under 3.3V supply voltage.

TABLE I. PERFORMACE SUMMARY OF THE PROPOSED PLL

TECHNOLOGY	0.35μm 2P4M CMOS
Supply Voltage	3.3V
Core Area	0.28×0.38mm^2
Operating Frequency Range	250MHz~1.29GHz
Cycle to Cycle Jitter	7.2ps
Long Term Jitter	16.6ps
Power @ 1.0GHz	38.2mW

VI. ACKNOWLEDGEMENT

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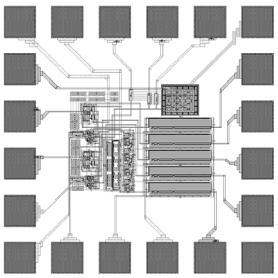

Figure 10. The chip layout.

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