# A Tunable Bandpass ΔΣ Modulator Using Double Sampling

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***Abstract*—A tunable switched-capacitor (SC) bandpass delta sigma (ΔΣ) modulator using double sampling by one input parameter is proposed. The center frequency of the modulator can be varied from fs/14 to 6fs/14 at a sampling frequency (fs) of 70MHz. Its performance can be hence improved by fine tuning the center frequency. The purposed modulator was implemented in 0.35-μm 2P4M CMOS standard technology with the core area of 4.2 mm$^2$. The measured dynamic range of 68dB within 200kHz bandwidth can be achieved. Its power consumption is 58mW under a 3.3-V supply voltage.**

## I. INTRODUCTION

A Bandpass ΔΣ modulators are widely used in intermediate frequency (IF) and radio frequency (RF) communication systems [1-3]. In order to avoid the low frequency noise in zero IF receiver and prevent the mismatch of the circuits from degrading the receiver performance, the single IF architecture is a good candidate as shown in Fig.1. Since the signal, which is received and down-converted, may be varied due to process variations, a tunable bandpass ΔΣ modulator is required to improve the performance of the receiver. There are so many efforts are devoted in tunable continuous-time (CT) ΔΣ modulator [4]-[5] by the modifying the transconductance of OTA in the resonator. However, an elaborate tuning scheme and an additional cost are demanded in the tunable continuous-time ΔΣ modulator.

Since the mismatch among capacitors is very small, the SC ΔΣ modulators are popular in narrow band data converter. In this paper, a tunable bandpass ΔΣ modulator by one parameter only [6] is adopted to optimize modulator performance. To achieve a tunable resonator in the modulator, a multiple path SC scheme is applied for the adjustments of the center frequency. A wide tuning range from fs/14 to 6fs/14 is preformed to demonstrate the flexibility of the modulator. Furthermore, a double sampling technique is used to relax the requirements of opamp performance.

In this paper, a tunable switched-capacitor bandpass ΔΣ modulator using double sampling and single input control is presented. In Section Ⅱ, the architectures of the resonator and the bandpass ΔΣ modulator are discussed. In Section Ⅲ, the circuit implementation of the modulator is described. Finally, The simulation results are discussed in Section Ⅳ.

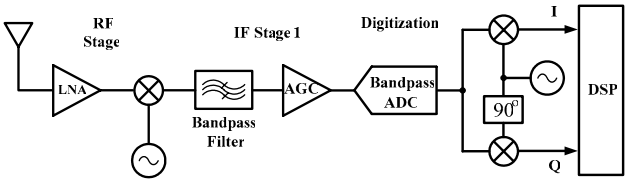



Figure 1. Single IF Receiver

## II. ACHITECTURE

### A. Algorithm

To transform a lowpass prototype to bandpass tunable modulator and keep the bandwidth from deviation in the transformation, the following relation can be applied [6]-[7]:

$$z^{-1} \rightarrow \frac{z^{-2} - \alpha z^{-1}}{\alpha z^{-1} - 1} \quad \text{and} \quad \alpha = \frac{\cos(\omega_c)}{\cos(B/2)} \tag{1}$$

where $\omega_c$ is the center frequency and $B$ is the bandwidth of the passband. The center frequency of the modulator can be adjusted by the different $\alpha$ values.

### B. Resonator

The tunable resonator is the basic function block in the presented bandpass ΔΣ modulator. Its transfer function $S_{TBP}(z)$ can be derived by applying (1) to $z^{-1}$ of $S_{LP}(z)$ as below:

$$S_{LP}(z) = \frac{z^{-1}}{1 - z^{-1}} \rightarrow S_{TBP}(z) = \frac{\alpha z^{-1} - z^{-2}}{1 - 2\alpha z^{-1} + z^{-2}} \tag{2}$$

By a simple derivation from the denominator of (2), the center frequency of the bandpass filter can be expressed as

$$f_{notch} = \frac{fs}{2\pi} ar\cos(\alpha) \tag{3}$$

For $\alpha$=0, the center frequency is located at one-fourth sampling frequency as that in the conventional bandpass ΔΣ modulator. For $\alpha$=±$n$, $n$ is a positive number, the center frequencies will be situated on symmetry positions respect to the one-fourth sampling frequency. A wider tuning range of the center frequency can hence be resulted. In this paper, two resonators are required to implement a fourth-order bandpass ΔΣ modulator, as shown in Fig. 2.

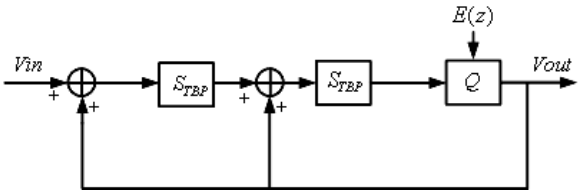



Figure 2. The architecture of the presented bandpass ΔΣ modulator

## III. CIRCUIT IMPLEMENTATION

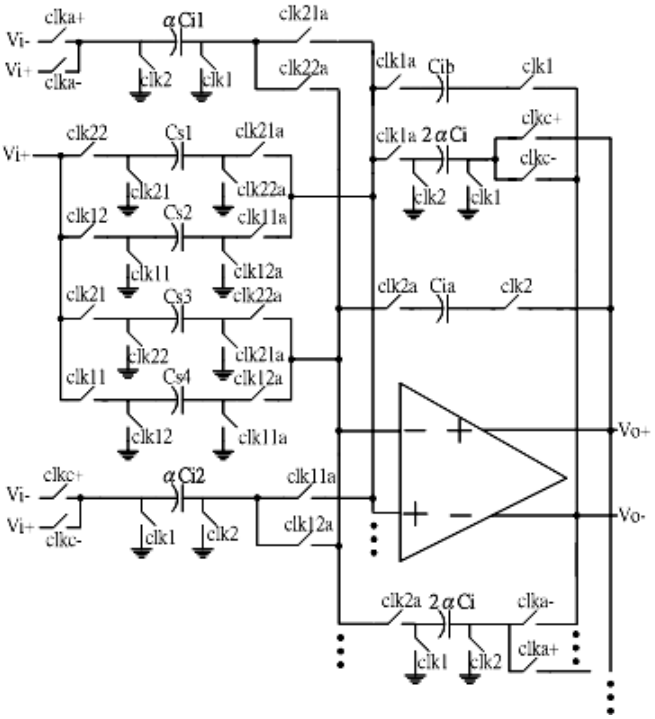
The presented tunable bandpass ΔΣ modulator consists of two tunable resonators and one 1-bit quantizer. The tunable resonator circuitry with double sampling technique [8-10] is drawn in Fig. 3. Its transfer function must be modified from (2) by replacing $z^{-1}$ with $z^{-1/2}$ :

$$S_{TBP}(z) = \frac{\alpha z^{-1/2} - z^{-1}}{1 - 2\alpha z^{-1/2} + z^{-1}} \tag{5}$$

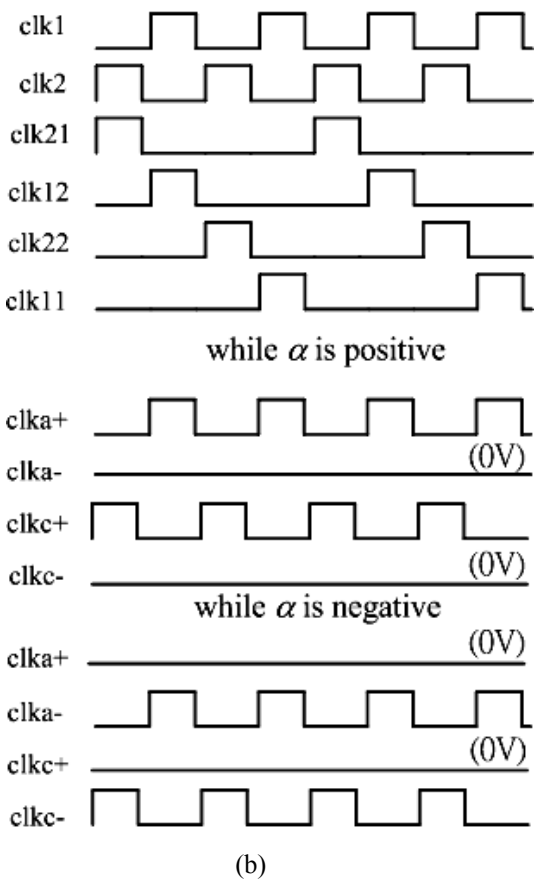
Thus, half the clock frequency can be obtained to relax the requirement of opamp.

The implementation of the tunable resonator with double sampling is depicted in Fig. 3(a). Here only half circuit is shown for simplicity. Six paths are required for the signal to realize the $z^{-1/2}$ and $z^{-1}$ terms in the nominator of (5). In order to obtain the positive and negative tuning coefficients $\alpha$ in the same resonator, two optional inputs, differential signals Vi+ and Vi–, are inserted in front of the sampling path, $\alpha$Ci1 and $\alpha$Ci2. One of the differential inputs can be selected by the different control signal clkc+ and clkc– in which the symbols "+" and "–" denote the sign of the $\alpha$ value. That is, the clocks clka+ and clkc+ are active while $\alpha$ is positive, and vice versa. Two feedback paths, both indicated by 2$\alpha$Ci, are required to keep the charge stored on the last half phase. There are two integrating capacitors, denoted by Cia and Cib, on differential output nodes for charge integrations in different phases, as drawn in the figure.

The operations are described in detail as follows. During the phase clk12, the input signals are sampled on the sampling paths, Cs3 and $\alpha$Ci2. In the phase clk11, the sampled signals on both the Cs2 and $\alpha$Ci2 together with the charge stored on the last half phase on the capacitor 2$\alpha$Ci2




(a)




(b)

Figure 3. (a) The presented resonator with tunable center frequency and (b) its corresponding clocks

are transferred to the integrating capacitor Cib. Note that the integrating capacitor on the negative output terminal is used in this integration to perform the transfer function of (5). Thus, the differential output of the tunable resonator will be turned over in the consecutive phases alternatively. Since the double sampling technique and the alternative output scheme are applied, there will be four distinct states are demanded to perform the operations of the tunable resonator. The corresponding clock phases are shown in Fig. 3(b). The clocks clk1a, clk2a, clk21a, clk12a, clk22a and clk11a are turned off slight early to reduce the charge injection effects. In this design, $\alpha$=0.9 is given and the capacitors Ci1=Ci2=Cia=Cib =Ci and Cs1=Cs2=Cs3=Cs4 are set.

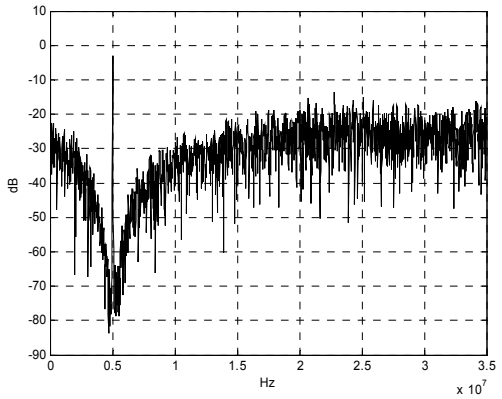
Since the heavy load and high operating frequency are driven in this design, the gain-boosted folded-cascode opamp [11] with the switched-capacitor common-mode feedback circuit [12] is adapted in the modulator. Two regenerative feedback comparators with latches [13] are used as the quantizers in two clock phases.

## IV. Simulation Results

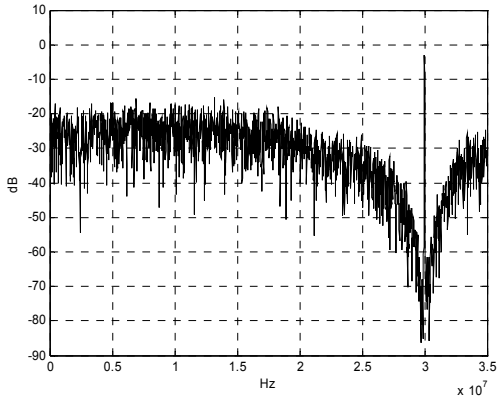
The presented tunable SC bandpass ΔΣ modulator using double sampling is simulated at 3.3-V supply voltage by HSPICE. The simulation results of the gain-boosted folded-cascode opamp are summarized in Table I. The positive and negative reference voltages are 1.9-V and 1.4-V, respectively. The clock frequency of 35MHz is used, and the effective sampling frequency of 70MHz can be got due to double sampling. From the simulation results, the output spectrum of the presented modulator with fin = 5MHz while $\alpha$=0.9 is chosen, as shown in Fig. 4(a). The output spectrum of the modulator with fin = 30MHz while $\alpha$=–0.9 is chosen, as shown in Fig. 4(b). It can be seen that the center frequency can be carried within a large range without altering the sampling frequency. The signal-to-noise ratio (SNR) of the modulator within 200kHz bandwidth under fin = 5MHz and fin=30MHz are 64dB and 60dB, respectively. The input dynamic range of 68 dB can be achieved. Fig. 5 shows simulated SNR versus input power in 200kHz bandwidth at the 70MHz of the sampling rate. The presented tunable SC bandpass ΔΣ modulator using double sampling is implemented in 0.35-μm 2P4M CMOS standard technology. Its layout is shown in Fig. 6. The core area of the modulator without PADs is 2.7*1.4μm$^2$. The power consumption is 58mW at 3.3-V supply. The performance of the modulator is summarized in Table II.

Table I. Summary of the Opamp Performance

| | |
|---|---|
| Process | 0.35um 2P4M standard process |
| DC gain | 82dB |
| Unity Gain Frequency | 423MHz |
| Phase Margin | 70 degree |
| Slew Rate | 163V/us |
| Load Capacitor | 5pF |
| Supply Voltage | 3.3V |
| Power Consumption | 22mW |




(a)




(b)

Figure 4. (a) The output spectrum of the proposed tunable SC bandpass ΔΣ modulator using double sampling for fin = 5MHz. (b) The output spectrum of the proposed tunable SC bandpass ΔΣ modulator using double sampling for fin = 30MHz.

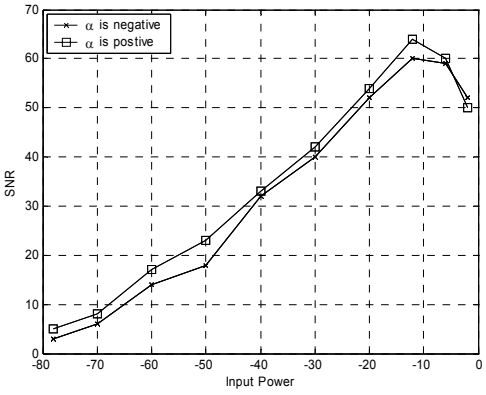



Figure 5. The SNR versus input power

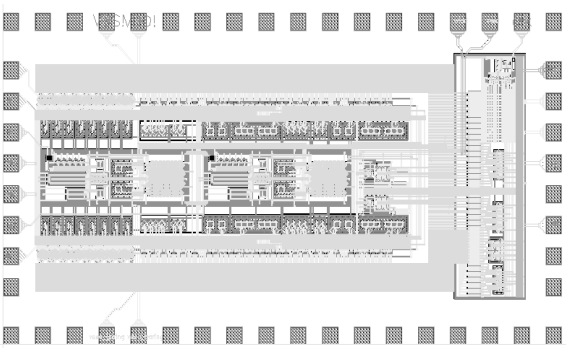


Figure 6. The layout of the modulator

Table II. Performance Summary of Tunable SC Bandpass ΔΣ Modulator Using Double Sampling

| | |
|---|---|
| Power Supply | 3.3V |
| Sampling Rate | 70MHz |
| Signal Bandwidth | 200kHz |
| SNR | 64dB |
| Dynamic Range | 68dB |
| Resolution | 11-Bit |
| Power Consumption | 58mW |
| Core Area | $2.8*1.5\mu m^2$ |
| Process | 0.35um 2P4M standard process |

## V. CONCLUSION

A tunable SC bandpass ΔΣ modulator using double sampling is presented in this paper. A wide tuning range of the center frequency demonstrates the feasibility of the tunable bandpass ΔΣ modulator by means of the distinct $\alpha$ value applied. The input dynamic range of 68 dB, which corresponds to 11-bit resolution, can be achieved. The presented modulator has been implemented in 0.35-μm 2P4M CMOS standard technology.


## ACKNOWLEDGMENT

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