A Novel Multimode Interference Optoelectronic AND Gate with Partial Index-Modulation Regions

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Abstract

A novel smart optoelectronic AND gate based on multimode interference structure has been proposed for the first time. Different from conventional methods, the multimode interference structure is employed to realize the AND logic function. It takes advantages of the linear operation and the easy-to-implement logic function. In this paper, the detailed investigations such as configuration of the logic gate, design rules of MMI structure and simulation results have been considered. Furthermore, the multi-input AND gate can be realized by cascading the following architectures.

1. Introduction

In recent years, broadband optical communication systems have attracted many researchers and stimulated great developments in high-speed optoelectronic logic gates. Much researches that focused on all-optical logic operations in photorefractive materials such as BaTiO3 crystals has been successfully completed in the near future [1-2]. In general, the most common used techniques for the optoelectronic logic gates were the nonlinear optical devices. Although these nonlinear operations have been successfully implemented by several methods, these methods still present some difficulties for practical considered.

In the past years, multimode interference (MMI) couplers have attracted considerable interest due to advantageous characteristics such as compactness, relaxed fabrication tolerance, polarization insensitivity, and large optical bandwidths [3]. MMI structures also have been found applications as variable-ratio power splitters and optimized switches [4-6], mode converters [7], and so on.

In this paper, we propose a novel structure for multimode interference optoelectronic AND gate. Difference from conventional method, the logic operation is controlled via phase modulation and it works as a linear device. By changing the refractive indices of the index-modulation region installed in the multimode waveguide, the AND logic function can be realized. Furthermore, the multi-input AND logic function also can be realized by cascading several AND gates.

2. Theory of multimode interference

The geometry of a general MMI with at most N possible input and N output guides is depicted in Fig. 1. For the mirror output j from the input i, the coupler length L is given by [8]

$$L = \frac{3 L \pi}{N} \qquad (1)$$

where N is the images of the input field, and $L\pi$ is the beat length of the two lowest-order modes, defined as[9]

$$L\pi = \frac{\pi}{\beta_0 - \beta_1} \cong \frac{4 n_{eff} W_{eq}^2}{3 \lambda} \qquad (2)$$

where n_{eff} means the effective refractive index, λ is the wavelength in vacuum, and W_{eq} is the equivalent MMI width.

To describe the phase modulation of MMI from Fig. 1, we split the MMI into three regions. The first and third regions are the free propagation regions. The second region is the phase modulation region by tuning the partial index at the middle of the MMI. It defines as

$$\Delta\phi_k = \frac{2\pi}{\lambda} \cdot \Delta n_{eff} \cdot L_{pad} \qquad (3)$$

where $\Delta\phi_k$ is the phase shifting of the modulated region, and L_{pad} is the modulated length.

3. Configuration of the optoelectronic AND gate

By applying the theories of GMMIs and partial index-modulation, the smart optoelectronic AND gate can be realized. The circuit configuration and truth table of the optoelectronic AND gate is shown in Fig. 2. The major configurations are composed of MMI switch, optoelectronic converters, and delay lines. The input power from the input B is applied to optoelectronic converter to modulate the partial input phase. The input signal from the input A will pass to the output waveguide if the partial index-modulation region is modulated by input signal B, and the signal will disperse to substrate without modulating the input phase. In addition, the purpose of the delay lines is to synchronize the optical and electrical signal in the MMI.

4. Circuits Layout and Simulation

After deciding the configuration of optoelectronic AND gate, the circuit layout and simulation can be completed. It shows as Fig. 2, the width and the length of the MMI waveguide are 8 μm and 531.65 μm, respectively. This means that the asymmetric input light is emitted from a cross port without any index modulation [8]. The length of the index-modulation regions are selected so as to obtain a phase change of π for a refractive index change of 1%. Furthermore, fundamental logic functions are analysed by the finite-difference beam propagation method (FD-BPM). The simulation results show in Fig.3 with the equivalent reflective index of the MMI waveguide and the substrate are 3.219 and 3.058, assuming an InGaAsP/InP ridge structure for λ=1.55 μm. From the Fig. 3(b), the output power is more than 99 percentage transferred, and the transferred power is less than 0.02 percentage in the Fig. 3(a).

5. Conclusion

In this paper, the novel optoelectronic AND gate has been proposed for the first time. It takes advantages of the linear operation and relaxed fabrication tolerance as compared to conventional methods. By phase modulation, the logic function would be easy to realize. Moreover, the high count port AND gates can be extend by cascaded architectures. Compared of the theory, BPM simulation shows good agreement, and based on these principles we can optimize the optoelectronic AND gate with simple steps.

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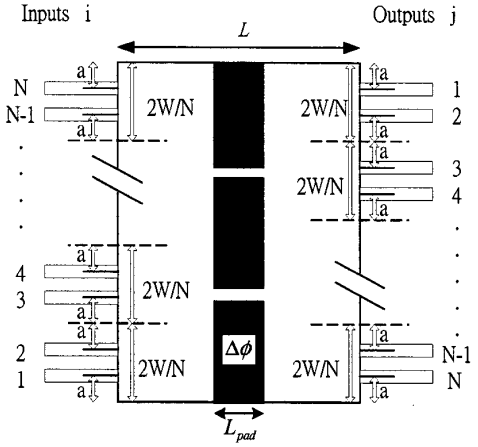
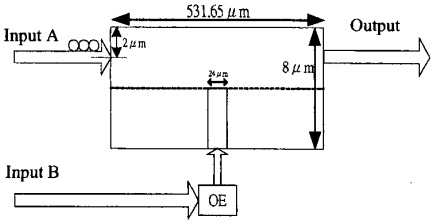


Fig. 1 The geometry of general MMIs with N possible input and N output guides. The shaded area means the phase modulation region.

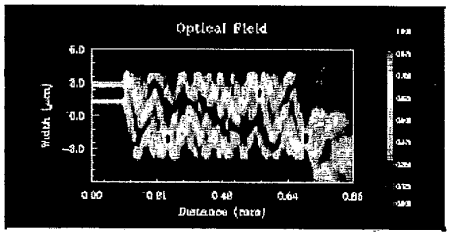


(a)

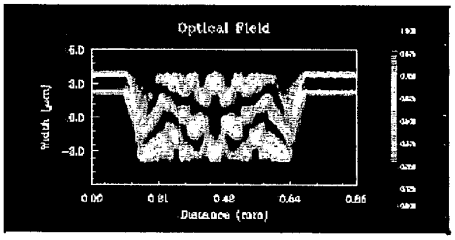
Input		Output
A	B	X
0	0	0
0	1	0
1	0	0
1	1	1

(b)

Fig. 2 The proposed optoelectronic AND gate:(a) circuit configuration and layout; (b) truth table



(a)



(b)

Fig. 3 The simulation results of the proposed optoelectronic AND gate with (a) the input logic function is 1 0; (b) the input logic function is 1 1.