The CMOS On-chip oscillator based on level Tracking Technique

Chia-Yang Chang	*Po-Chang Chen*	*Ching-Yang Yang*	*Yang-Han Lee*
graduate student	graduate student	associate professor	associate professor
789350054@s89.tku.edu.tw	689350121@s89.tku.edu.tw	ycyang@huafan.hfu.edu.tw	yhlee@ee.tku.edu.tw

ABSTRACT In this paper, we propose the architecture of a CMOS Fully integrated level-locked loop (LLL). A 455KHz LLL without external reference signal achieves the target of 1 percent variation, and consumes 9mW with 3.6V power supply in standard 0.5μm CMOS process. The frequency-to-voltage converter (FVC) in LLL built upon charge redistribution principle can decrease the variation of process. A programmable controller is developed to increase the frequency accuracy. The voltage- controlled oscillator (VCO) is based on differential delay cells in order to minimize the effect of the power supply and the substrate noise. According to main circuits operate in 1.8 V provided by regulator, the output frequency is accurately on 455KHz from 2.0V to 3.6V.

Index Term — PLL, FVC, VCO

I INTRODUCTION

A phase-locked loop (PLL) circuit is a modern interesting electronic building block widely usage in electronics and remote access system (RAS), especially in many integrated application. It is implementation in automatic control systems of frequency or phase such as communications, frequency synthesis, clock generation, clock recovery, radar, cellphone and instrumentation system. The PLL circuit generates an output signal that tracks an input reference signal. The output signal is synchronized with the input reference signal in frequency as well as in phase. Usually, a PLL is built around a phase frequency detector (PFD),a charge pump, a low-pass filter and a voltage- controlled oscillator (VCO) or current-controlled oscillator [1]. The PLL may also include frequency dividers and mixers when used in synthesizing frequency applications [2] [3]. The low-pass filter is required to ensure the stability and to determine the bandwidth of the PLL by filtering the PFD output signal. Typically, the low-pass filter is not integrated but implemented externally with discrete components in order to minimize the area of the integrated PLL. To overcome these design constraints and to allow the circuit to be fully integrated with an acceptable die area, we propose, in this paper, a level-locked loop (LLL) similar to a PLL in the way that it generates an output signal which tracks an input reference signal [4] [5].

However, in this case , the output signal is synchronized only in voltage level with the input signal and not in phase or in frequency , therefore the locking time of this LLL would be very short. The LLL is based on a new architecture that does not require the use of the phase detector and the charge-pump. The proposed LLL contains a frequency-to-voltage converter (FVC), an active low-pass filter, a bandgap, a regulator, a differential voltage-controlled oscillator (VCO), a scaling circuit, a delay-element, a divider and a programmable controller. The proposed LLL is mainly a negative feedback circuit and the architecture is shown in Fig.1. The FVC circuit in LLL generates a feedback voltage signal ,Vfed that tracks a reference voltage signal , Vref provided by Regulator. Moreover the LLL will have a fixed output frequency when Vfed is equal to Vref, as shown in Fig. 2. Based on the operation principle, the programmable controller is added to select the output frequency. In other words, the value which Vfed is equal to Vref can be select to design the output frequency met the target.

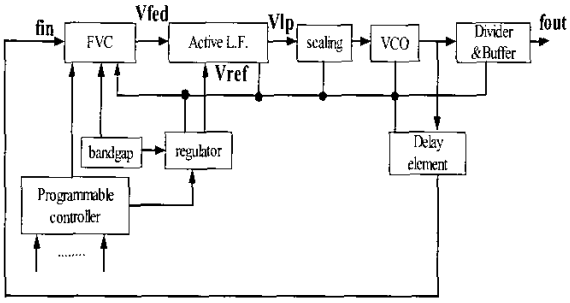


Fig. 1 Block diagram of the LLL circuit

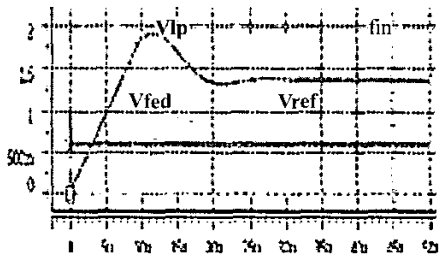


Fig. 2 Simulation results of the LLL

0-7803-7363-4/02/$17.00 ©2002 IEEE

Ⅱ Circuit Description and Simulation

The operation principle of LLL is based on voltage comparison of a reference and feedback signal which instead of phase comparison, and where voltage comparison is completed by combining a FVC and an active filter. It is generally used in systems involving a programmable controller to reduce the process variation and to target 1 percent variation on 455KHz. The main circuits operate in 1.8V provided by a regulator which needs a steady reference voltage provided by Bandgap , and the reference voltage is independent of Vdd as shown in Fig.3

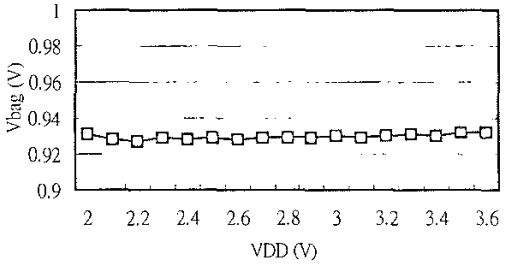


Fig.3 The output voltage of bandgap

1. Frequency-to-Voltage Converter (FVC)

The architecture of this FVC is built upon the charge redistribution principle based on switching capacitors, and requires control signals that are derived from its input signal [6]~[8]. The FVC technique is used extensively to realize the monolith frequency synthesizer with fractional multiplication form the LLL because of its easy implementation and high accuracy.

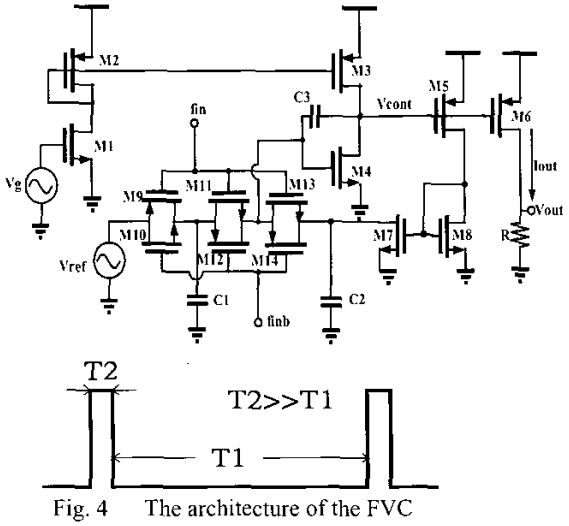


Fig. 4 The architecture of the FVC and the input frequency

As shown in Fig.4, the output voltage of the integrator controls the current ***gmVcont*** which discharge C2 during phase 1, of duration T1, while C1 charges to Vref. During phase 2, of duration T2, C1 and C2 connected to the virtual ground at potential Vg. The transconductance ***gm*** is determined by M5 and the mirror ratio ***N=(W/L)8/(W/L)7***. The charge Q=C1 (Vref-Vg) lost by C1 flows into C2 and C3. The steady state is established when the charge received by C3 is 0 so that Q flows entirely in the storage capacitance C2. Charge balance in C2, at steady state, imposes Q=Im7*T1 thus:

$$Im_7=C1*(Vref-Vg)/T1 \qquad ...(1)$$

The current of M5 is proportional to the Iout and from (1), the equation (1) can be written by

$$Vout=R*N*C1*(Vref-Vg)/T1 \qquad ...(2)$$

when ***(W/L)5*** is equal to ***(W/L)6***. According to the input frequency of FVC must fit a condition of T1 is larger than T2 as shown in Fig.4, the delay circuit is added to change the duty cycle of VCO. Because the vdd provided by regulator is 1.8V and the use of standard 0.5μm CMOS process, the use of transmission gate is to decrease the resistance and redistributes charge fully in the switch system M9 to M14. By the equation (2), the output voltage is proportional to the pulse of frequency *f1* (1/T1) as the value of Vref , Vg , C1 , R is fixed. From the simulation result as shown in Fig.5, it proves the Vout is proportional to *f1* no matter what kind of parameter in 0.5μm CMOS process.

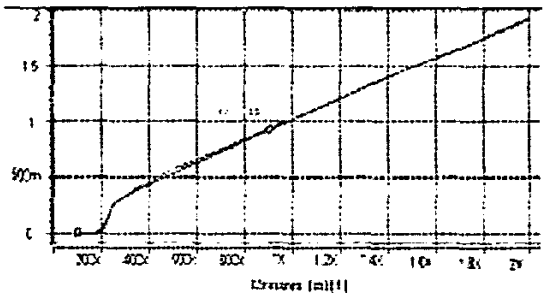


Fig.5 the characteristic of FVC

2. Voltage-Controlled-Oscillator (VCO) and Differential-to-Single-Ended Converter

The four-stage VCO uses differential elements with PMOS cross-coupled loads, as shown in Fig. 6. The cross-coupled load is composed of symmetric load of M6~M9 with cross-coupling of M4~M5. The symmetric load has an characteristic of I-V curve is symmetric, and which provides differential-mode resister that is independent of common-mode voltage carrying the supply noise. Although the symmetric load with real MOS device can not maintain linearity, symmetric load can also be used for achieving high dynamic supply noise rejection [9][10]. From the noise point of view, the cross-coupling mos of M4~

M5 can increase the symmetry of load and reduce the phase noise [11]. The mos of M4 and M5 exhibits a negative resistance of $-2/gm$, which increase the output impedance and lower the frequency of oscillation [12]. By the way , the oscillation frequency of VCO just can be down to 910KHz.

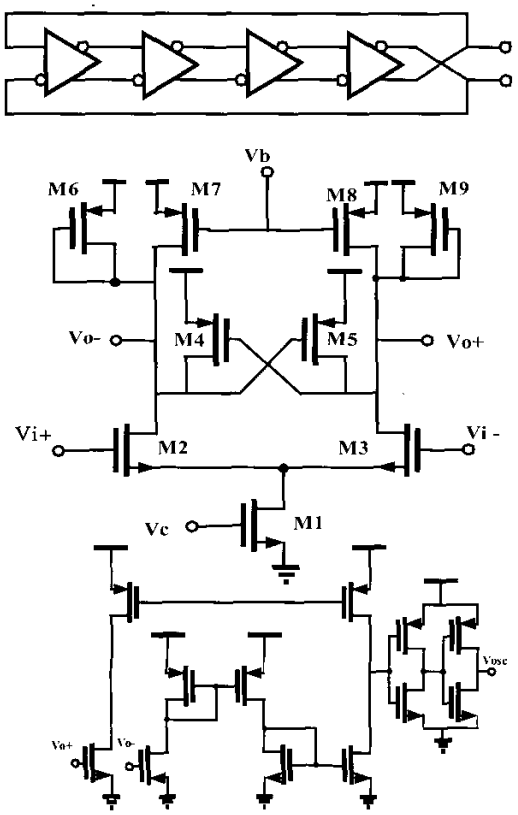


Fig. 6 Schematic of the VCO, differential cell and differential-to-single-ended converter

The differential-to-single-ended converter, divider and output buffer is connected behind the VCO in sequence. The differential-to-single-ended converter is composed of two NMOS common-source amplifiers connected by two PMOS current mirror and a NMOS current mirror. The NMOS common-source amplify the differential signal of VCO and convert to a single-ended output through the NMOS current. Furthermore the two inverter is added to make output signal full swing. The output buffer is necessary to isolate the VCO from the other sub-blocks that require the VCO outputs and to provide enough power to drive high-capacitive loads without disturbing the VCO operation.

3 Active Filter and Scaling circuit

In many broadband tuning applications, it is necessary to supply a higher tuning voltage that the LLL similar to the PLL is allowed to create. The active filter is composed of an opamp, resisters and capacitors as shown in Fig. 7. The opamp is used for comparing the voltage, Vfed from the FVC and the voltage, Vref from the regulator. In other words, the opamp is used to realize a comparator. Although the input offset of opamp will introduce error, the programmable controller can revise it. The resisters and capacitors are used for filtering the switching noise introduce from FVC and controlling the poles on the loop [13]. Additionally, the reason for using an active filter is typically to get an increased tuning voltage of the VCO [14].

The scaling circuit is connected between active filter and VCO as shown in Fig. 7. If Vfed is larger than Vref, the output voltage of the active filter is low. Further, the scaling circuit turns the low voltage into the tuning voltage range which VCO can oscillate. And then, the lower frequency oscillation by VCO results in the lower voltage output of the FVC. By the negative feedback loop the output frequency will keep steady when Vfed is equal to Vref.

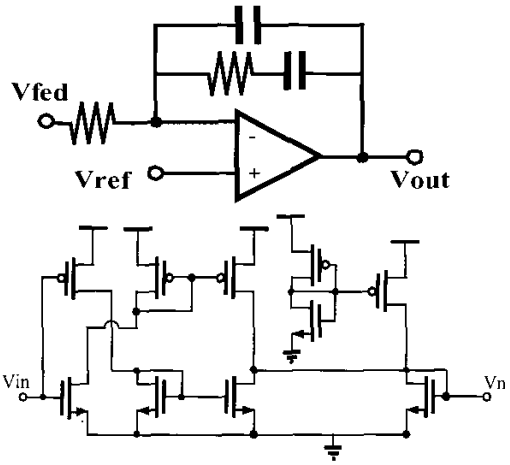


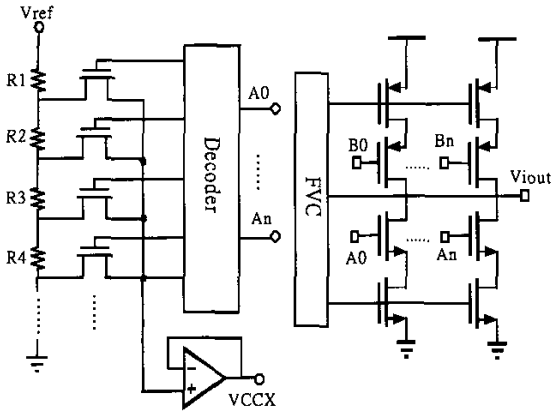
Fig. 7 Schematic of the Active filter and Scaling circuit

4 Programmable Controller

The programmable controller is included of two parts which develop to increase the accuracy of output frequency as shown in Fig. 8. First, the resister-string D/A converter is used to select the Vref provided by regulator. From the simulation results at TT-condition shown in Fig. 9. Each code has averagely a shift frequency of 30KHz and the dynamic range is about 450KHz. Second, the current-mode converter is used to control the output voltage, Vfed of FVC. The Fig. 9 shows that each code has averagely a shift frequency of 5KHz. From the frequency shift of view, the first part is called the coarse tuning; oppositely, the second part is called the fine tuning. This thesis proposed four codes in coarse tuning part and three codes in fine tuning part. However the accuracy of the frequency and the tuning dynamic range is dependent on the

programmable controller which supports how many codes.

Fig.8 Schematic of the Programmable controller



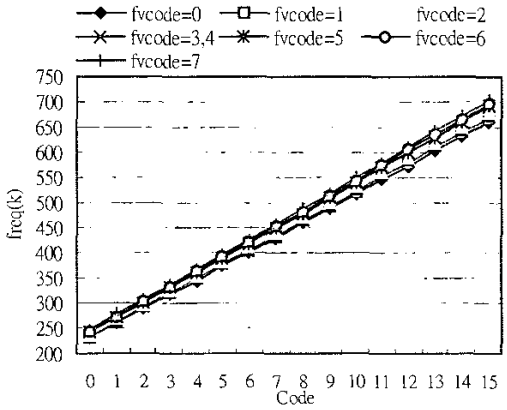


Fig. 9 The distribution of the output frequency

Ⅲ Conclusion

The on-chip 455KHz oscillator with a programmable controller based-on level tracking technique is proposed and simulated in standard 0.5μm CMOS process. According to the power supply of FVC, VCO, Active filter, and Scaling circuit is 1.8V provided by the regulator , the output frequency is on 455KHz from 2V~3.6V. Because of the process has variation so that the programmable controller is added to increase the accuracy of the output frequency. The parameter of the on-chip oscillator is listed in Table 1.

Table 1. Electrical characteristics

Supply voltage	3.6V
Power consumption	9-mW
Frequency output	455KHz+4.5KHz
Process	0.5μm CMOS
Workable Voltage range	2.0V~3.6V

Reference

[1] R. E. Best, "Phase-Locked Loops: Theory, Design and Applications." New York McGraw-Hill, 1984.

[2] V. V. Kaenel, D. .Aebischer, C. Piguet, and E. Dijkstra, "A 320 MHz, 1.5mW @ 1.35V CMOS PLL for microprocessor clock generation, "IEEE J. Solid-State Circuits, vol. 31,pp. 1715-1722,Nov. 1996.

[3] D. .L. Chen, "A power and area efficient CMOS clock /data recovery circuit for high-speed serial interfaces, "IEEE J. .Solid-State Circuits, vol.31, pp.1170-1176,Aug.1996.

[4] A. .Djemouai, M.Sawan, and M.Slamani, "New circuit techniques based on a high performance frequency-to-voltage conversing, " presented at the IEEE Int. Conf. Electronics Circuits and Systems, Pafos, Cyprus, 1999,pp.13-16.

[5] A. .Djemouai, M.Sawan, and M.Slamani,"A200 MHz frequency-locked loop based on new frequency-to-voltage converters approach ," presented at the IEEE Int. Symp. Circuits and Systems, Orlando, FL, 1999, pp.1189-1192.

[6] A. .Djemouai, M.Sawan, and M.Slamani, "High performance integrated CMOS frequency-to-voltage converter, "presented at he Int Conf. Microelectronics, Monastir, Tunisia, 1998, pp. 63-66.

[7] A. Djemouai, M.Sawan, and M.Slamani, "New frequency-Locked Loop Based on CMOS frequency-to-voltage Converter Design and Implementation " IEEE Transactions on circuits and systems, vol.48, NO. 5, MAY 2001

[8] A. Mortara, E. Vittoz and P. Heim "Simple PFM Demodulator to be used by Analogue Artificial Neural Networks which Communicate through Pulses" Electronics Letter Feb. 1993

[9] John G. Maneatis and Mark A. Horowitz, "Precise Delay Generation Using Coupled Oscillators" IEEE J. .Solid-State Circuits, vol. 28,NO.12 DEC 1993

[10] John G. Maneatis , "Low-Jitter Process-Independent DLL and PLL Based on self-Bias Techniques" IEEE J. .Solid-State Circuits, vol.31,NO.11 NOV 1996

[11] Rafael J.Betancourt-Zamora and Thomas H. Lee, "CMOS VCOs for Frequency Synthesis in Wireless Biotelemetry", ISLPED98, Monterey, CA.USA@ 1998 ACM 1-58113-059-719810008

[12] Rehzad Razavi, "Design of Analog CMOS Integrated Circuits", Published by McGraw-Hill, 2001.

[13] William F. Egan, "Phase-Lock Basics", Wiley-Interscience publication

[14] PLL Performance, Simulation, and Design National Semiconductor p.89~100.