Design of Optical Decoder and Optical Address Translator for High Speed Optical Switching Network

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0.1 Abstract

In this paper, we will study the key technologies for the high speed optical switching network using the optical header/payload discriminator, optical decoder and optical address translator for header recognition, decoding and translating addresses directly in the optical domain.

This system utilizes the optical ring resonator (ORR) for header/payload discriminator (OHPD). We design the optical delay line decoder (ODLD) and translator (OTR) for decoding and translating optical address for routing control. For ODLD, we will design the hierarchical prime code structure with delay line logic to increase the channel capacity. For OTR, we will design the optimal code mapping algorithm, and serial or parallel code architectures.

1 Introduction

Optoelectronic switching technology is very promising for high speed optical switching network [1]. Many switching architectures are limited by the electronic switching speed. Therefore it is very important to investigate optical switching technologies for the future high speed optical backbone network.

In this paper, we will study the key technologies for the optical cell switching network. This system uses the optical ring resonator (ORR) for header/payload discriminator (OHPD). We design the optical delay line decoder for decoding address directly in the optical domain for routing control. The proposed high speed optical switching system utilizes the time-slot-interchange (TSI) technology [2] to directly translate the address in the optical domain as the optical header address translation. Therefore, the routing control in the header can be processed in the optical domain and the payload can be optically switched to the destination output.

In order to increase the throughput of this optical network, we can apply the laser array and optical amplifier as wavelength converter for high speed optical switch based on wavelength division multiplexing.

2 System Description

The optical packet switching network is shown in Fig.1. The header of the incoming packet goes into the header processor which multiplexes the playload and header. The header processor uses the delay line decoder (DLD) as an optical correlator [3] for routing control. And the optical address information in the header can be changed for the next optical switching nodes with the time-slot-interchange (TSI) [2] technology to directly translate the header in the optical domain for the next stage switch. The configuration of the header processor with decoder and translator are shown in Fig.2.

We consider the optical network system based on cell switching . Each cell makes up of header and playload. The header has the information for routing control which can be processed in the optical domain. The playload carries the data information which can be switched to the destination output.

The header of the incoming cell goes into the header processor which multiplexes the playload and header. The header processor uses the delay line decoder (DLD) as optical correlator [3] for virtual path indicator (VPI) / virtual channel indicator (VCI) routing control. In the asynchronous transfer mode (ATM), the VPI/VCI should be changed for the next optical switching nodes. Here we apply the time-slot-interchange (TSI) [2] technology to directly translate the header in the optical domain for the next stage switch. The configuration of the header processor with the VVDLD (VPI/VCI Delay Line Decoder) and VVTR (VPI/VCI Translator) are shown in Fig.2. The VVDLD's generates the electrical control signals which also control the E/O switch for choosing the corresponding map translator code.

3 Analysis

We design VVDLD for decoding address directly in optical domain for routing control and utilize the hierarchical prime code structure to increase the channel capacity as shown in Fig.3. This hierarchical prime code structure combines the prime code of 7 (P7) together with the prime of 3 (P3). We propose the al-

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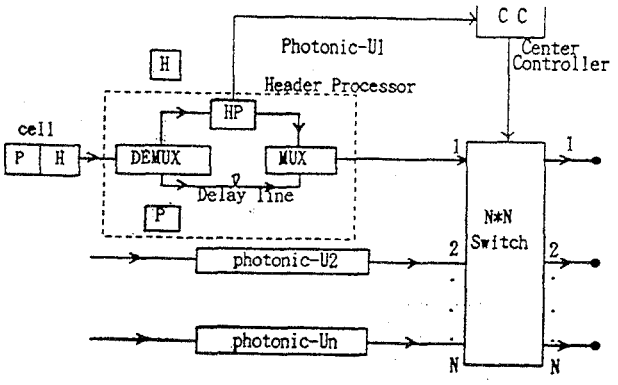

Fig.1 A Generic Optical Switch Structure

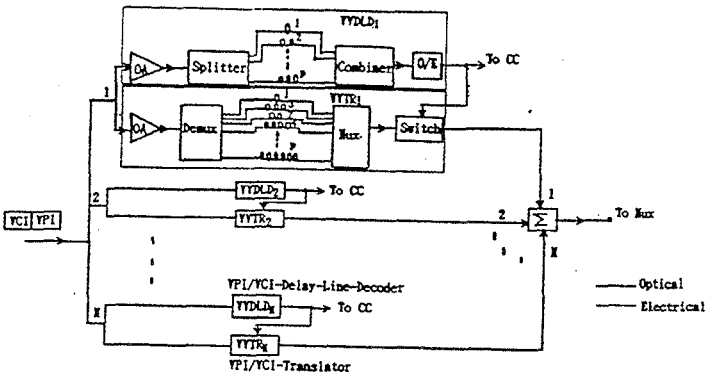

Fig.2 Configuration of the HD(Header Processor) using YYDLD(YPI/YCI-Delay-Line-Decoder) and YYTR(YPI/YCI-Translator)

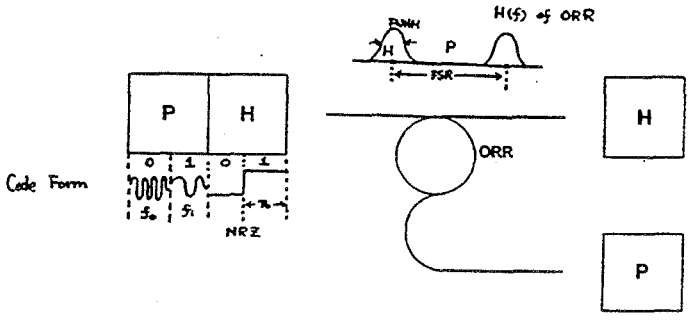

Fig. 4 Optical Header / Payload Discriminator

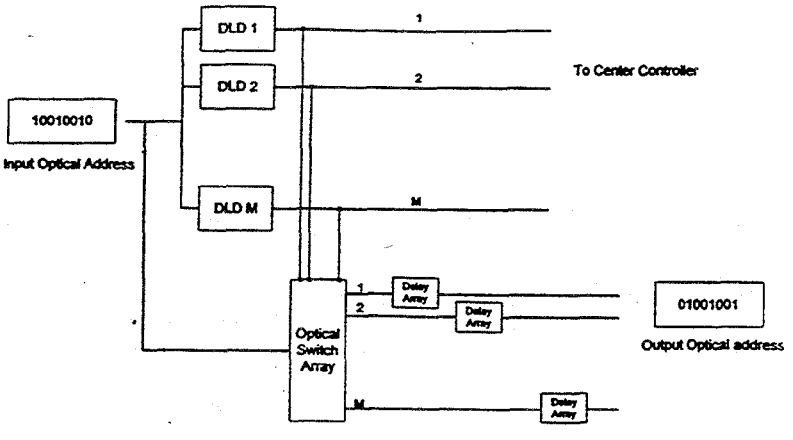

Fig. 5(a) Block Diagram of Optical Address Translator (OATR)

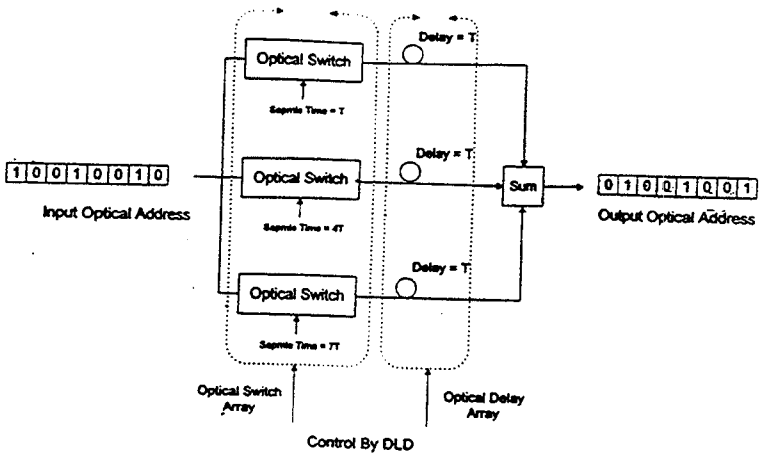

Fig. 5(b) Configuration of Optical Address Translator (OATR)

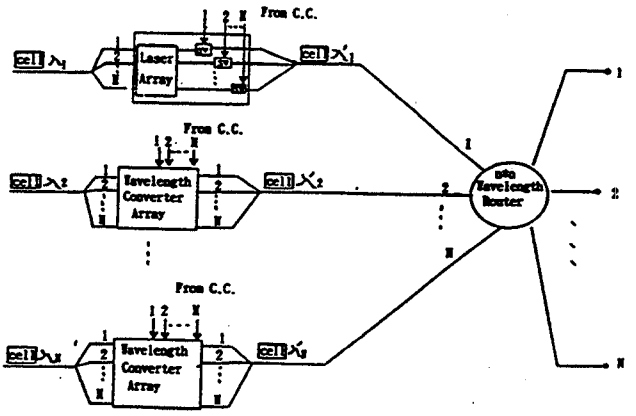

Fig.6. N×N WDM Switch Based on Laser Array as Wavelength Converter

gorithm for designing this hierarchical code structure and find the optimal decision position (ODP) for the decoder as shown in Table-I.

The header with the control information uses the baseband NRZ codeform and the payload with the data information uses the binary FSK modulation as shown in Fig.4. Therefore, we can design the transfer function, H(f), of the optical ring resonator (ORR) as, FWHM $\geq$ Rb, FSR $\geq$ FWHM+2Rb+Δf where Rb is the data rate, Δf is the frequency deviation, and FWHM is the full wave half maximum of the ORR.

We design optical address translator for the optical header address translation (OATR) in the optical domain for the next switch as shown in Fig.5. The input optical address can be changed by the optical switch array according to the optimal code mapping algorithm and criterion as shown in Fig.5(a). In Fig.5(b), we have shown the example for mapping the input code of 10010010 into the output code of 01001001 with the optical switch array at the sample time of T, 4T, 7T with the optical delay array at the same corresponding delay of T.

We utilize the wavelength converter together with the wavelength router for implementation of wavelength division multiplexing as shown in Fig.6 to improve the throughtput of the proposed optical network.

4 Conclusion

In this paper, we have studied the key technologies for the high speed optical switching network using the optical header/payload discriminator, optical decoder and optical address translator for header recognition, decoding and translating address directly in the optical domain.

This system utilizes the optical ring resonator (ORR) for header/payload discriminator (OHPD). We design the optical delay line decoder (ODLD) and translator (OTR) for decoding and translating optical address for routing control. For ODLD, we will design the hierarchical prime code structure with delay line logic to increase the channel capacity from P^2 to $500P^2$. For OTR, we will design the optimal code mapping algorithm, and serial or parallel code architectures.

Acknowledgements

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References

[1] J.W., Lockwood, et. al., "Scalable Optoelectronic ATM Networks : , The IPOINT Fully Functional Testbed," Journal of Lightwave Technol., vol.13, no.6, pp.1093-1103, 1995.

[2] S. Kuwano, et. al. "Optical FDM/TDM Cross-connect Employing a Self-Dulplex Light Source and an Optical Time Slot Interchange," Elect. Lett., vol.30, no.11, pp.878-879,1994.

[3] T. O'Farrel, et. al., "Switched Correlator Receiver Architecture for Optical CDMA Networks with Bipolar Capacity," Elect. Lett., vol.31, no.11, pp.905-906,1995.

[4] W.C. Kwong, et. al., "2N Prime-sequence code and its optical CDMA coding architecture," Elect. Lett., vol.30, no.6, pp.509-510,1994.