A 3.3V ALL DIGITAL PHASE-LOCKED LOOP WITH SMALL DCO HARDWARE AND FAST PHASE LOCK [#]

Jen-Shiun Chiang and Kuang-Yuan Chen [*]

Department of Electrical Engineering
Tamkang University
Tamsui, Taipei, Taiwan

ABSTRACT

This paper is to design and implement an all digital phase-locked loop (ADPLL) circuit. The core of the ADPLL is the switch-tuning digital control oscillator (DCO). Our design of the DCO has features of small hardware cost. This ADPLL has characteristics of fast frequency locking, full digitization, easy design and implementation, and good stability. It is suitable to be used as the clock generator for high performance microprocessors. A prototype of this ADPLL chip is designed and implemented by TSMC's 0.6um SPDM CMOS process. The simulation shows that this chip can operate in the range between 60MHz and 400MHz, and operates at 4x the reference clock frequency. The phase lock process is 47 clock cycles, and the phase error is less than 0.1ns. The chip consists of 4026 MOS transistors and the core size of the VLSI layout is 923um × 921um.

1. INTRODUCTION

The PLL has been designed for application and integration on high clock-frequency microprocessors. It can eliminate the delay between external and internal clock caused by the on-chip clock driver delay. This delay causes large setup and hold time for the input and output signals and is a limitation on the design of systems at high clock frequency. The analog PLL traditionally fills this target [1-5]. However, integrating a PLL on a microprocessor chip is difficult because of the noise. Integrating an analog circuit on a die with digital circuits has a large amount of generated digital noise[6-8]. To overcome such problems, the all digital phase-locked loop (ADPLL) is proposed [9-11]. The ADPLL has characteristics of fast frequency locking, fully digitization, and good stability.

This paper describes a modified ADPLL. The core of ADPLL is the switching-tuning digital control oscillator (DCO). This DCO is implemented by controlling the different MOS switches to get different frequencies. The key elements of the implementation of the DCO are with four modes and 14-bit of binary weighted control, with the accuracy of 2-cycle frequency comparator, a control unit which controls the system operation, and a phase detector. It saves half layout area than the traditional DCO (compared to [10]). The ADPLL is composed of frequency comparator, phase detector, control unit, and our proposed DCO. The phase-locked procedures for this ADPLL are frequency acquisition, phase acquisition, and frequency and phase maintenance respectively. In the frequency acquisition mode, a binary search algorithm is used to capture the frequency. In the phase acquisition mode, the bit-shifted method is applied to align the phase. In frequency and phase maintenance modes, a special algorithm is adopted to maintain the required frequency and phase. The performance of the ADPLL circuit is a 47-cycle phase lock; the oscillator frequency is more than 400MHz, and the phase error is less than 0.1ns (at 200MHz).

The remaining of this paper is organized as follows. Section 2 introduces the architecture of the ADPLL. Section 3 describes the whole circuit design such as frequency comparator, phase detector, control unit, and DCO. Simulation results of this chip are provided in Section 4. Finally, concluding remarks are given to conclude this paper in Section 5.

2. ARCHITECTURE OF THE ADPLL

The phase-locked procedures for this ADPLL are frequency acquisition, phase acquisition, frequency maintenance and phase maintenance respectively. Figure 1 depicts a block diagram of the ADPLL. The control unit contains the DCO control register which dictates the frequency of the DCO. Arithmetically incrementing or decrementing the DCO control word modulates the DCO frequency and phase.

Phase lock procedures begin at the frequency acquisition mode. At this mode a binary search algorithm sweeps the DCO frequency range (divide by 4) to match that of the reference clock. The algorithm changes the DCO control word based on the output of the frequency comparator. When frequency acquisition is completed, the ADPLL enters the phase acquisition mode. A bit-shift method is applied to align the phase. The ADPLL increments or decrements the DCO control word until the phase detector senses a change in the phase polarity of the reference relative to the internal clock. The value held by the phase-gain register dictates the magnitude of the changes to the DCO control word in phase acquisition mode. Phase acquisition is finished when the phase detector senses the phase change in polarity. At the end of phase acquisition, the ADPLL transfers the DCO control word which defines the baseline frequency to the anchor register. Then the ADPLL enters phase maintenance and frequency maintenance modes. In phase maintenance made the ADPLL increments or decrements the DCO control word every reference clock based on the output

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* Kuang-Yuan Chen is with Key Tech Coporation, Science Based Industrial Park, Hsin Chu, Taiwan.

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of the phase detector, unless the phase polarity changes from that of the prior cycle. When the phase polarity changes, the contents of the anchor register are transferred to the control register to restore the baseline frequency. In the frequency maintenance mode, the ADPLL will increment or decrement the contents of the anchor register and the baseline frequency is thus changed.

3. CIRCUIT DESIGN

3.1 Digital Control Oscillator (DCO)

The heart of the ADPLL is DCO. Like most voltage controlled oscillator, the DCO consists of a frequency-control mechanism with an oscillator block. There are two parameters to modulate the frequency of the ring oscillator. One is the propagation delay time of the inverter, and the other is the total number of the inverters. The traditional DCO tunes the first parameter, but the second one is ignored [10]. Our proposed switch-tuning DCO is shown in Figure 2. Each inverter is cascaded with 14-bit control MOS devices. The sizing ratio of the control devices is 2x as shown in Figure 2(a). The most significant control bit, bit 13, corresponds to the largest control device, whose dimension (W × L) is 256um × 1um. The DCO architecture is shown in Figure 2(b). We insert the CMOS transmission gate or inverter cascadely to the neighbors of the cells. Thus we can change the total stage of the ring oscillator by choosing one transmission gate ON and others OFF. The size of the layout area is reduced compared to the traditional DCO.

3.2 Frequency Comparator

The frequency comparator accepts the reference clock and the DCO outputs as inputs. By these two inputs it generates two mutually exclusive signals, "fast" and "slow", and an enable signal, "Enable" for the DCO. The "Enable" signal forces the reference clock edge and the DCO output edge to align in phase. The comparator takes one-half reference cycle for synchronization before asserting "slow" or "fast". In the remaining of the reference clock, the DCO is disabled. Therefore, a complete frequency comparator iteration needs two reference clock cycles.

Figure 3 shows a block diagram of the frequency comparator, and Figure 4 shows a timing diagram of two frequency comparator iterations. The first rising edge of the reference clock enables the DCO and starts to count the DCO output; the second rising edge of reference clock captures the output of the DCO divider (divide by 4) which is the input to the synchronizer. If the output of the DCO divider arrives before the second rising edge of the reference clock, then the DCO output is defined as "fast". Conversely, if the output of the DCO divider arrives after the second rising edge of the reference clock, then the DCO output is defined as "slow". After synchronization, the frequency comparator generates a "fast" or "slow" signal, and disables the DCO. The circuit of the match delay matches the delay in enabling the DCO and the delay in the DCO divider. If the frequency of the DCO (divide 4) identically matched the frequency of the reference clock, then both the signal and the synchronizer clock arrive concurrently at the same rising time. The match delay may decide the accuracy of the frequency comparator.

3.3 Phase Detector

The phase detector aligns the DCO clock edge to the reference clock edge. It is important to notice that the DCO clock differs from the DCO output in that it is phase aligned to the internal microprocessor. In practice, there are several stages of logic separating the DCO clock from the DCO output. It contains two series-connected edge-triggered D flip-flops and auxiliary logic blocks. The two flip-flops are clocked by the reference clock and its complement respectively and the flip-flops receive the DCO output as inputs. The auxiliary logic block outputs an "ahead" or "behind" signal based on the output of the flip-flops.

The phase detector provides no information about the phase-error magnitude. Instead it provides the relative direction of errors. There exists a situation that a false detection in phase polarity can occur. The situation arises when the initial phase error between DCO clock and reference clock is 180 degrees. In this situation, noise can induce a change in phase polarity and indicate false phase alignment. Inserting a divide-by-two circuit between DCO clock and reference clock can improve it. Figure 5 shows the timing diagram of the phase detector. When the first rising edge of the reference arrives, the flip-flop locks the output of the DCO_DIV2 (high). When the first falling edge of the reference arrives, the output of the phase detector is "ahead". When the second rising edge of the reference arrives, the flip-flop locks the output of the DCO_DIV2 (low). When the second falling edge of the reference arrives, the output of the phase detector is "behind".

3.4 Control Unit

The control unit accepts the results of frequency comparator and phase detector results as inputs and changes the mode signals and control word signals of the DCO. Figure 6 shows the block diagram of the control unit. In frequency acquisition mode, we first adjust the mode of the DCO by the algorithm of Figure 7. It needs 2-4 iterations to find the correct mode. Then we use the binary search algorithm to adjust the control word. At the beginning a pointer register points to the most significant bit of the frequency register. If the frequency comparator asserts "fast", the pointed bit changes to "0". Conversely, if the frequency comparator asserts "slow", the pointed bit changes to "0" and the last pointed bit changes to "1". The value is stored to DCO control word register. The pointer moves to the next bit. When the pointer register value is equal to "0", the ADPLL enters the phase acquisition mode. It takes 16-18 iterations to finish this mode.

In phase acquisition mode, the output of the phase detector decides the DCO control word. The phase-gain register contains a bit-shift (8 bit to the right) value of the binary DCO control word. If the phase detector asserts "ahead", the ADPLL transfers the adder output to the DCO control register. Conversely, if the

phase detector asserts "behind", the ADPLL transfers the subtractor output to the DCO control register. This event increments or decrements the DCO control word by the value in the phase-gain register. When the phase polarity is changed, phase acquisition is finished and the ADPLL transfers the DCO register to the anchor as baseline frequency. It takes at most 11 reference cycles to finish this mode. The phase lock process at most needs 47 reference cycles.

When the phase lock process completes, a maintenance mode begins. The ADPLL enters the phase maintenance and frequency maintenance modes. In frequency maintenance mode, an algorithm maintains the baseline frequency. The ADPLL saves the DCO control register to the anchor register whenever four consecutive cycles without a change in phase polarity occur. If the phase polarity is changed, the ADPLL restores the anchor register to the DCO control register. In phase maintenance mode, an algorithm adjusts phase-gain register. When the phase polarity is changed, the phase-gain value divides by 2. The phase-gain value is multiplied by 2 whenever the ADPLL detects eight consecutive incremental change in the same direction. The algorithm iterates as necessary.

4. THE IMPLEMENTATION AND SIMULATION

Since the design is an all-digital implementation, we design and simulate this ADPLL in a digital simulation environment. A standard RTL simulator, Verilog, is the primary digital simulation tool and it helps us to prove our design. We build our own 3.3V cell library, and finish the VLSI layout by Cadence's auto place and route (APR) tool. The ADPLL implementation requires 4026 transistors and $923\mu m \times 921\mu m$ in a TSMC $0.6\,\mu m$ CMOS process. The layout of this chip is shown in Figure 8. The DCO runs up to 400MHz with a supply voltage of 3.3V. At 200 MHz, the ADPLL achieves a less than 0.1ns skew-to reference. The phase-lock process at most needs 47 cycles.

5. CONCLUSION

An improved ADPLL is proposed in this paper. The RTL simulator of Verilog gives us sufficient information to design a working circuit. It can save a lot of design time compared to an analog PLL circuit design. We also propose a new DCO. The main advantage is that it takes much less hardware cost compared to the traditional DCO. The prototype of this ADPLL chip is implemented by TSMC's 0.6um SPDM CMOS process. The HSPICE simulation and Verilog simulation shows that this chip could operate in the range of 60MHz to 400 MHz, and operate at 4x the reference clock cycles. The phase error is less than 0.1ns and the phase-lock process is 47 clock cycles. The lock time of this ADPLL is much faster than the analog PLL circuits.

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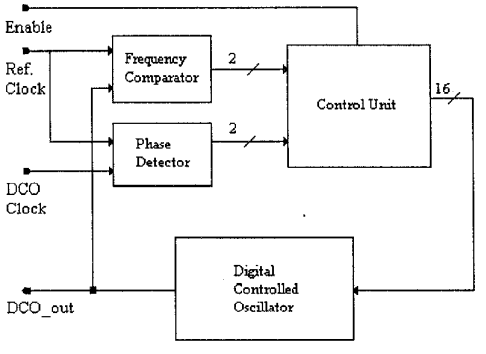
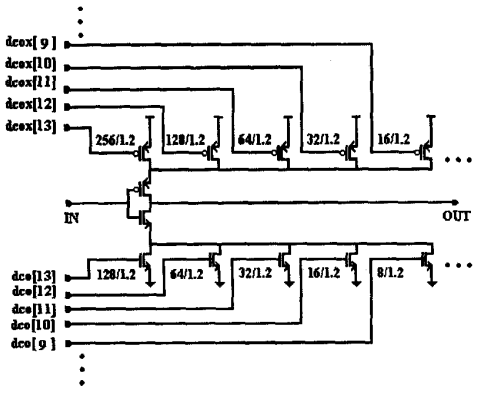
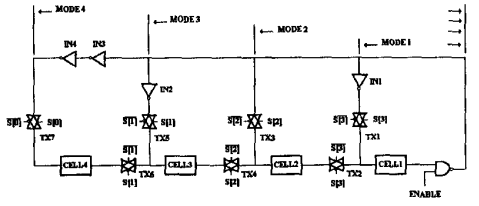


Figure 1. ADPLL Block Diagram



(a) the DCO Cell



(b) the DCO

Figure 2. The Proposed DCO Architecture

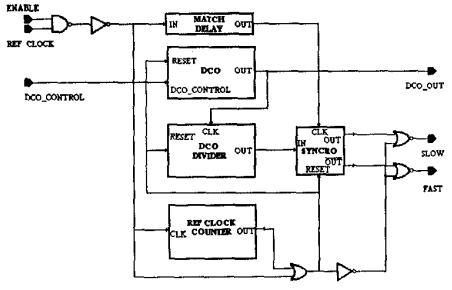


Figure 3. The Frequency Comparator

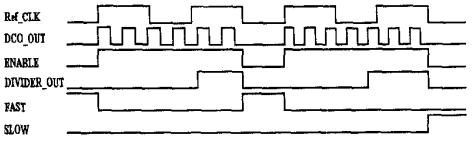


Figure 4. Timing Diagram of the Frequency Comparator

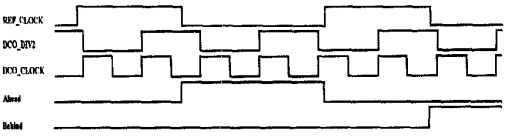


Figure 5. Timing Diagram of the phase detector

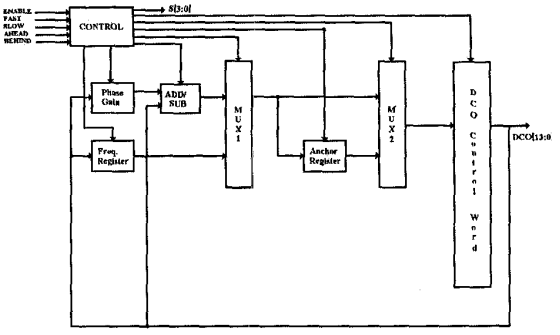


Figure 6. The Block Diagram of the Control Unit

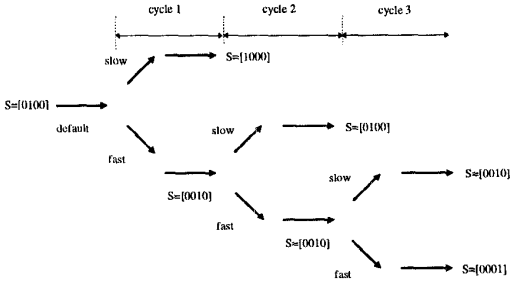


Figure 7. The Algorithm of the DCO Mode

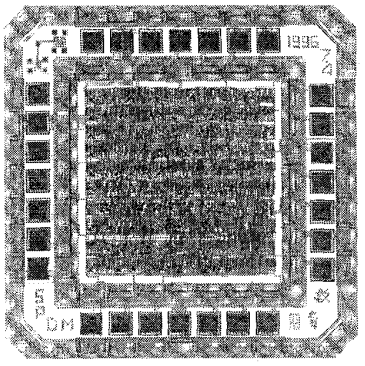


Figure 8. Chip Layout of the ADPLL