A New CMOS Current-Sensing Complementary Pass-Transistor Logic(CSCPTL) for High-Speed Low-Voltage Applications

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Abstract

In this paper, a new pass-transistor logic called the current-sensing complementary pass-transistor logic tree (CSCPTL) is proposed and investigated. The new logic circuit can be used in the low-voltage low-power system for high-speed applications. To exam the low-voltage applications, a 1.2V supply voltage. is selected for one battery back-up systems. The current-sensing scheme yields a good sensing speed in small voltage swing than voltage sensing. But the dc power dissipation problem of the current mode circuit make it difficult to apply in low power applications. The new circuit can resolve the dc power problem in current-sensing scheme. The new circuit has superior speed performance with a power-delay product compared to LCPL which is acknowledged to have the most potential in low-voltage low-power digital circuits design. The CSCPTL can be operated at 1.2V without changing conventional 5V CMOS process.

I. Introduction

Micropower integrated circuits are the key to the realization of portable electrical system. The main techniques to reduce the power consumption in the circuit level are the capacitance minimization on logic tree and supply voltage reduction [1], [2]. In generally, power supply scaled-down is the most efficient method to realize power reduction of digital circuits. Obviously, it makes the circuit delay increased. A technique to improve the circuit delay for low-power systems is to reduce the threshold voltage Vt. But reduction of threshold voltage increasing the MOS subthreshold leakage current [3].

Many logic families and sensing scheme, the CVSL logic, DCVSL logic [4], improved Domino Logic [5], Current Steering Logic (CSL) [6], DCVSPG [7] and CPL [8], [9] are proposed to yield a fast access time and reduce the power dissipation. However, all these logic families do not keep their advantages at low supply voltage. Some of them can not work if Vdd < (Vtn+Vtp). Among the proposed logic circuits, CPL is recognized to have potential in low power digital circuit design. But CPL does not keep the speed performance on low-voltage operation due to the delivered voltage from NMOS CPL logic tree is only Vdd-Vtn (body effect), that could be less than 400mV at 1.2V power supply applications. Thus the input slop from multiple NMOS in series is slow. It increases the short circuit power Pdc at cross-coupled PMOS latch.

In view of those advantages and disadvantages, a new digital circuit called Current-sensing Complementary Pass-Transistor (CSCPTL) is proposed. The CSCPTL operated at 1.2V supply voltage without changing the standard process for 5V logic circuits. The new circuit using the concept of sensing the small voltage swing in DRAM chip [10] to improve the access time, and utilizing the characteristic of the half capacitance in CPL compared to conventional CMOS. It is shown that CSCPTL is 2.2 times faster than static LCPL and of 40% improvement in maximum operating frequency for dynamic circuit.

II. Static CSCPTL and Dynamic CSCPTL (SCSCPTL & DCSCPTL)

The CPL is taken to be the trend on low-power digital circuit design because of the half capacitance thus saving 1/2 transient power and 2 times fast than conventional CMOS digital circuits. The basic concept of CPL circuit is shown in Fig. 1. Conventionally, LCPL utilizing a PMOS cross-coupled latch to regenerate signal from CPL logic tree and two static inverter to drive next stage as shown in Fig. 2. But it's maximum operating frequency was limited to latch regeneration at slow output data transient of the latch node.

In this paper, a current-sensing complementary pass-transistor logic (CSCPTL) was proposed to improve the operation speed. The CSCPTL has two versions, the

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static and the dynamic CSCPTL. It is shown that the new circuits has no dc power dissipation.

A. static CSCPTL

The circuit diagram of the static CSCPTL is shown in Fig. 3. If Inb=0 and In=1, PMOS MP1 and MP3 will be turned on and MP2, MP4 are turned off. Then node S1 starting to be charged by MP1, S2 to be discharged because MP4 is off and MN5 is still on. Thus makes MN3 to be turned off because S2 getting low. In the same time, MN5 is turned off by S2(low). By inserting two NMOS MN5, MN6 in the master part of the sense-amplifier, the dc current in the conducting path of master part is cut after storage node S1 S2 changes state. Fig. 4 shows that the current in the path Ibo is cut off effectively after transient of the master part in this current sense-amplifier was finished. Hence there is no dc power dissipation. And the output is then charged to be high by MP3. In the same time, outputb is changing it's state to be low by MN2 because S1 is charged by MP1. From Fig. 5, the node S1 and S2 turn to be transient was shown, the output is soon to be stable.

When transient operation of SCSCPTL, the sensing speed is a function of PMOS dimension ratio. To have better speed performance, the dimensions of the PMOS are optimized to be 2-3 times of NMOS CPL logic tree. If the dimension of PMOS is too large, then the speed will degrade because of larger capacitance loading of CPL logic tree. In contract, small PMOS dimension produces fast transient but smaller pull up current. And the dimensions of output NMOS influences the pull down speed.

B. dynamic CSCPTL (DCSCPTL)

In many applications, there needed a higher operating clock rate to meet system performance. Though we can use architecture level, (e.g. double hardware for parallelism to get about 2 times throughput, thus double power) to enhance system performance, a faster circuit is still preferred in the advantage of a simple data path and circuit complexity thus chip area.

The schematic diagram of the dynamic CSCPTL was shown in Fig. 5(a). It has no dc power dissipation as the static CSCPTL does. The basic concept of the dynamic CSCPTL is similar to static CSCPTL but adding two clocked NMOS MN7 and MN8 between CPL logic tree and current sensing circuit to control the signal passing from CPL logic tree. The sense node is pre-charged to high to minimize the leakage in hold cycle.

As ck=1, the dynamic CSCPTL shown in Fig. 5(a) is operated in the pre-charge phase. Node A and B are pre-charged to 500mV. All the PMOS are cut-off, thus there has no dc power in this phase. As ck=0, the dynamic CSCPTL is operated in the evaluation phase. MN7 and MN8 are turned on, nodes A and B are conditionally discharged by the CPL tree. Conventionally, the dynamic circuit is pre-charged to Vdd by PMOS but that leads to a longer delay to discharge in evaluate phase. In this thesis, the circuit pre-charge to 500mV instead of 1.2V. The circuit speed performance hence improved.

The pipelined connection of the dynamic CSCPTL is shown in Fig. 5(b). The circuit and the corresponding clocking of the ϕ-stage is shown in Fig. 5(a). The $\bar{\phi}$-stage is similar to that of the ϕ-stage with the clock signal *ck* is replaced by $\overline{ck}$ and the $\overline{ck}$ is replaced by *ck*. The ϕ-stage and $\bar{\phi}$-stage are connected alternately to form the pipelined connection.

III. Simulation Results of CSCPTL and Comparison to LCPL

The CPL is proposed to operate at a double operating speed than conventional CMOS circuit with smaller power consumption. By canceling the PMOS in the logic tree thus provides a good power-delay product among digital circuit. And is also suitable in low power low voltage design. The proposed circuits are also for low voltage micropower with higher speed than LCPL. Fig. 6 and Fig. 7 shows the gate delay and power-delay product comparisons of the static CSCPTL and LCPL with variation fan-in number respectively. Fig. 8 shows the maximum operation frequency comparisons of the dynamic CSCPTL and LCPL with variation fan-in number. Fig. 9 shows the power consumption comparisons of the dynamic CSCPTL and LCPL with variation operating frequency. The SPICE simulation results are based upon the 0.8 μm single-poly double-metal n-well CMOS process.

As showed in Fig. 6, the delay time of static CSCPTL is at only 45% in comparison to LCPL at 1.2V power supply. And Fig. 7 shows the power-delay product of static CSCPTL is about 1.2 times compared to LCPL. It illustrates that the static CSCPTL can be gained a double operating speed by increasing a tolerable power-delay product. From the Fig. 8, the dynamic CSCPTL was operated at a faster frequency compared to LCPL 1.40 times with the fan-in from 3 up to 12. Fig. 9 shows the power consumption of dynamic CSCPTL and LCPL with variation operating frequency. It is shown that the power is proportional to operating frequency such indicates the proposed circuit has no dc power problem. The new proposed micropower circuit can be operated for high-speed applications at 1.2V with a tolerable power.

IV. Conclusion

A new circuit (CSCPTL) was proposed for high-speed low-voltage low-power applications. It enables the transfer time of CSCPTL to be shorter than LCPL. The static and dynamic CSCPTL were proposed in this paper.

The static CSCPTL achieves 45% delay time at 1.2V power supply in comparison to LCPL, and a 40% improvement in maximum operation frequency for dynamic circuit. It was confirmed that the CSCPTL circuit allows to low-voltage high-speed operation. The current-sensing scheme combined with CPL logic tree is better than conventional voltage mode CPL buffer in small voltage swing for low-voltage operation to achieve higher speed.

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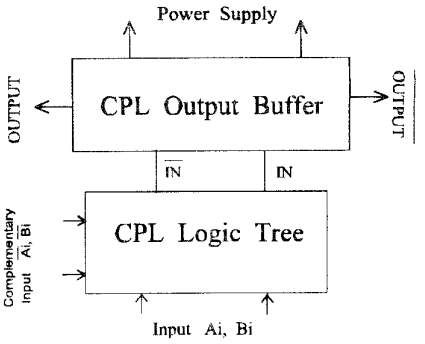

Fig.1 The Block Diagram of CPL Circuit

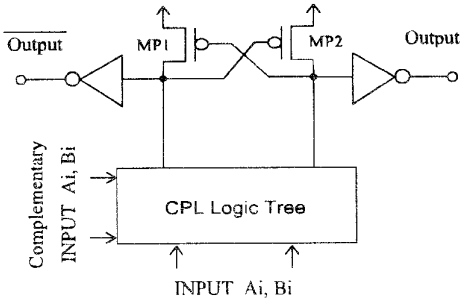

Fig.2 The LCPL Circuit Diagram

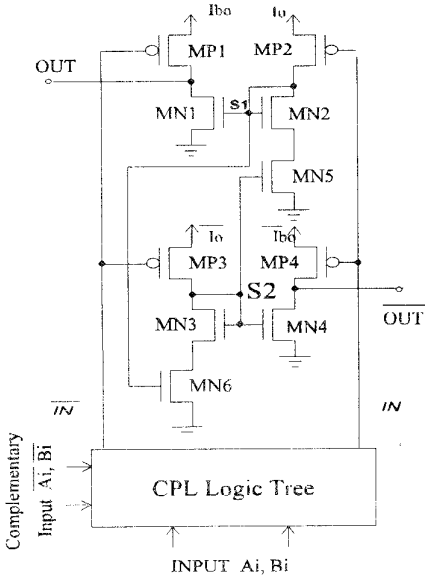

Fig.3 The Circuit Diagram of Static CSCPTL

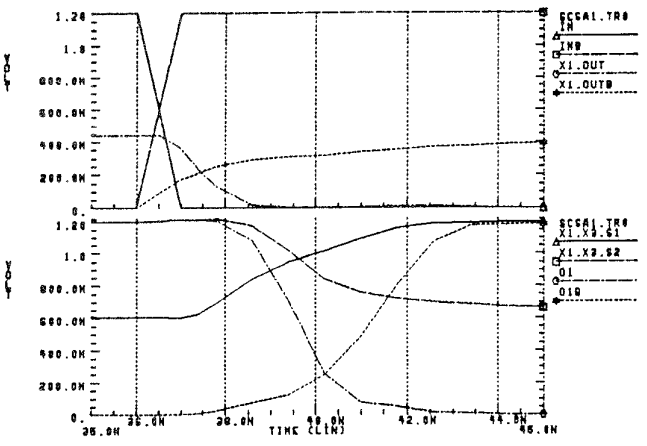

Fig.4 The SPICE Simulation Results on CSCPTL, X1.OUT= NODE B, X1.OUTB = NODE A

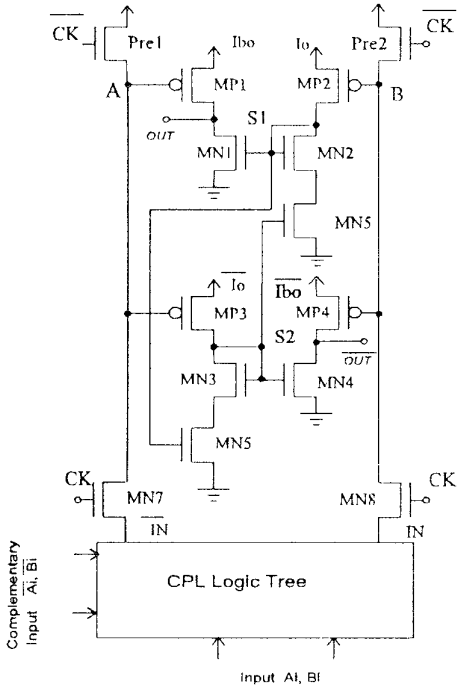

Fig.5(a) The Dynamic CSCPTL Circuit, ϕ -Stages

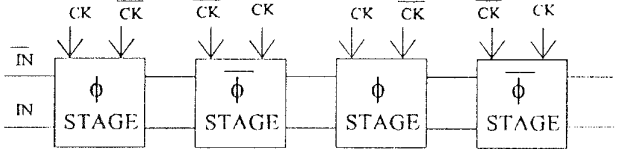

Fig.5(b) Pipelined connection of dynamic CSCPTL

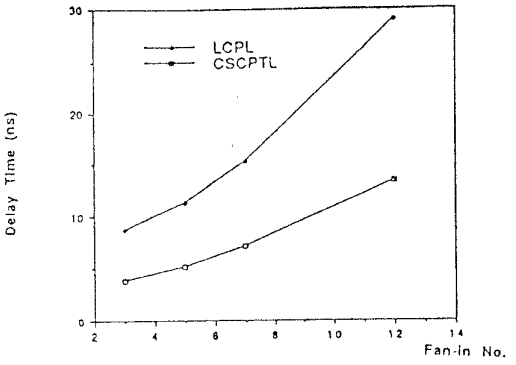

Fig.6 The Circuit Delay vs. Fan-in NO. between Static CSCPTL & LCPL

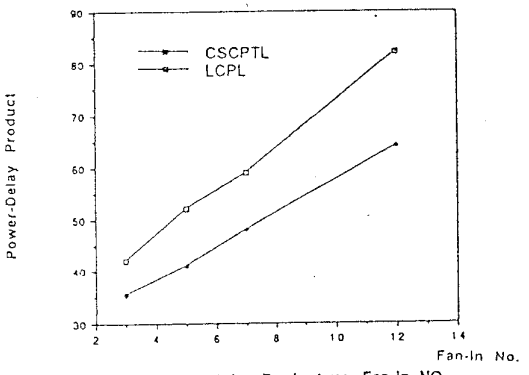

Fig.7 The Power-Delay Product vs. Fan-in NO. between Static CSCPTL & LCPL

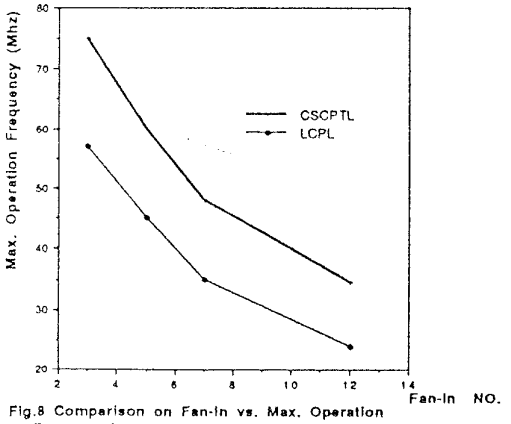

Fig.8 Comparison on Fan-in vs. Max. Operation Frequeny between CSCPTL & LCPL at 1.2V

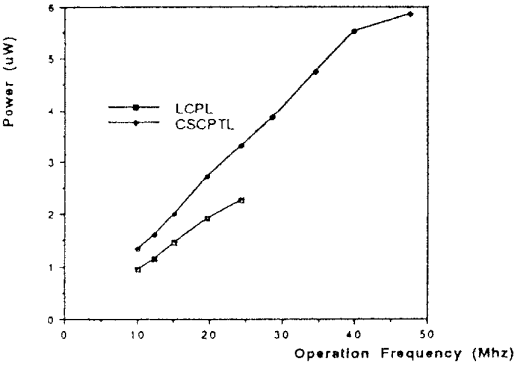

Fig.9 Frequency vs. Power on CSCPTL & LCPL with Fan-in Variation at 1.2V Power Supply