MICRO PRESSURE SENSORS OF 50μM SIZE FABRICATED BY A STANDARD CMOS FOUNDRY AND A NOVEL POST PROCESS

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ABSTRACT

This paper describes a piezoresistive micro pressure sensor with a size of 50μm made by a standard CMOS foundry and a novel post process. The material of the sensor diaphragm is silicon dioxide, and the piezoresistors are made by polysilicon. For releasing the diaphragms of the micro pressure sensors, this work proposes to use the front-side etching technique with etching holes of 5μm×5μm only. Finally, we use one of the protein stuffs, gelatin, to seal the etching holes. The sensitivity of the piezoresistive pressure sensor is 8.56±0.13 mV/V/psi.

1. INTRODUCTION

In recent years, CMOS-based microsensors benefit from the well-established IC fabrication technologies and the possibility of on-chip circuitry. Many sensors and actuators including thermal sensors, pressure sensors, tactile sensors, accelerometers [1-3], and even micromotors [4] had been made successfully. In these devices, the implemented on-chip circuitry can provide functionalities of calibration, self testing, and having digital interfaces. It revealed that MEMS technology using CMOS foundry process is a feasible and a convenient approach.

Although a mature CMOS foundry ensures the process reliability and shortens the developing time of microsensors, it still has some technical limitations. A client must follow the fixed fabrication process and the strict design rules during his R&D stage of MEMS devices fitting to a specific purpose. In our research, for example, we'd like to utilize the front-side etching instead of the back-side etching process to release a pressure diaphragm structure for the reason of reducing the sensor size substantially, as shown in Fig. 1. To meet this need, we must adjust our CMOS MEMS design and process in many ways. We not only have to design proper materials and configuration for sacrificial layers and the sealing stuff, but should also consider the appropriate process flow for releasing the sacrificial layers and for sealing the pressure cavities as well.

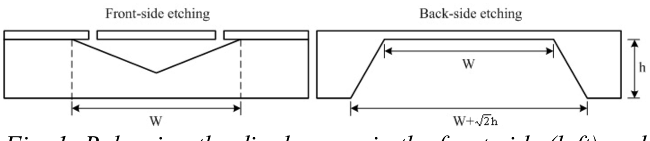

Fig. 1: Releasing the diaphragm via the front-side (left) and the back-side (right) etching methods by using KOH.

2. DESIGN PRINCIPLE

Piezoresistive pressure sensor

In this work, four polysilicon piezoresisors on the oxide diaphragm are connected as a Wheatstone bridge to sense the pressure. The location of the piezoresistors, shown in Fig. 2, was assigned on the diaphragm edge according to the conventional design of pressure sensors. Polysilicon is chosen to make piezoresistors because it's the only candidate having obvious piezoresistive effect among the available CMOS materials provided by commercial IC fab.

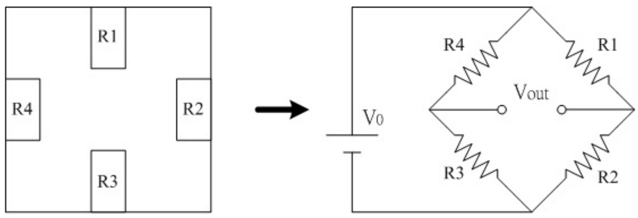

Fig. 2 Arrangement of piezoresistors

CMOS foundry process

A CMOS foundry of TSMC 0.35μm 2P4M (2-poly-4-metal) process, provided by CIC (Chip Implementation Center), Taiwan, is used in this work. Fig. 3 is the cross-section view of a CMOS pressure diaphragm with the nonplanar configuration of an inverted seashell herein.

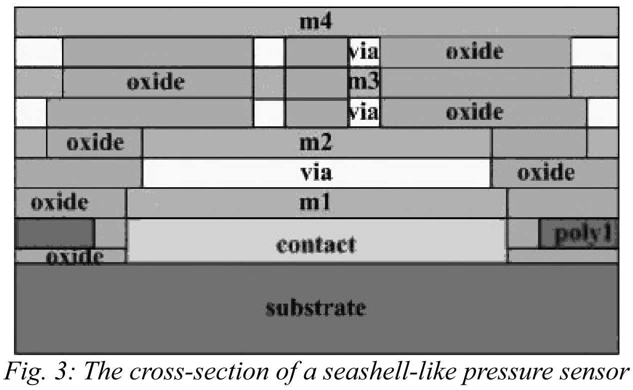

Fig. 3: The cross-section of a seashell-like pressure sensor depicting the layers stacked by the CMOS 2p4m process.

The "contact" layer made by Ti-W, the "via" made by Ti-W, and the "metal" made by aluminum, are all assigned as the sacrificial layers. The SiO_2 occupies all the interstitial space of the above three kinds of metal layers is then novelly assigned as a non-planar seashell-like sensing diaphragm for a pressure sensor, as shown in Fig. 4. There are 16 sensors arranged as a 4×4 array in a completed chip in Fig. 5.

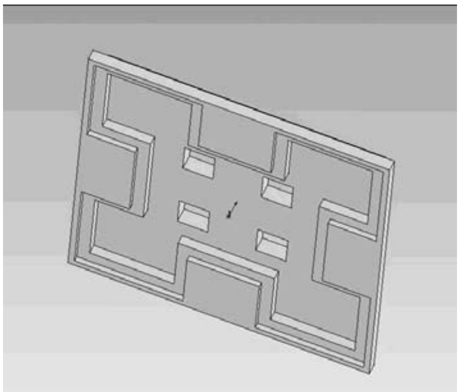

Fig. 4: Backside view of a seashell-like pressure diaphragm made of SiO_2 with 4 etching holes.

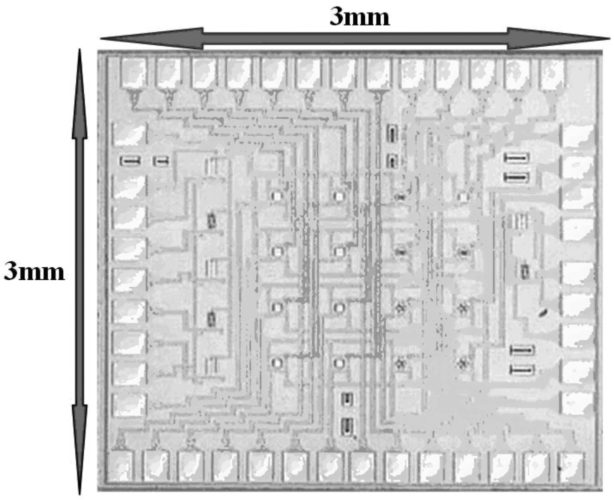

Fig. 5: CMOS pressure sensor-array chip after IC foundry.

Figs. 3 and 4 reveal the non-planar characteristic of our pressure diaphragm structure. Furthermore, an X-shape metal sacrificial pattern was designed intentionally to inlay the 4 polysilicon piezoresistors into a square diaphragm domain. The purpose of the above tentative design is proposed to overcome the difficulty of making CMOS pressure sensors proceeded by the front-side post etching.

Conventionally, the piezoresistors made by polysilicon are strictly arranged near the bottom of an oxide diaphragm. Such a stacking sequence of CMOS layers cannot be altered due to the strict design rules. If we want to free-stand the diaphragm portion preserved with piezoresistors, an undercut by KOH anisotropic etching underneath the piezoresistors (protected by gate SiO_2) is necessary. This is why we design the X-shape metal sacrificial layers. In addition, for not causing the large thickness or huge stiffness of SiO_2 diaphragm covering the piezoresistors so as to guarantee the good pressure sensitivity, a non-planar, inverted seashell-like diaphragm structure instead of a traditional flat diaphragm is made. Finally, we design the etching holes as small as 5μm×5μm only, for keeping the completeness and fair mechanical strength of the non-planar diaphragm.

3. POST PROCESS

Front-side etching

We chose high selective etchants listed in Table 1 to remove different sacrificial layers [5] including "contact", "metal" and "via". Etchant #A is used to etch the Ti-W alloy (the "contact" and "via" layers.) Etchant #B is used to remove the aluminum (the "metal" layer.) The sacrificial layers etching process is shown as follows: First, we clean the CMOS pressure sensor die with the acetone, IPA and D.I. water. Second, the die is immersed in etchant #B maintained at 70℃ for 50 minutes. Third, the die is immersed in etchant #A maintained at 70℃ for 30 minutes. We repeat the second and third steps for five times to remove the sacrificial metal layers clearly. The X-shape sacrificial spacer composed of the above metal layers disappears and exposes the silicon substrate after the front-side etching. The silicon anisotropic etching #C finally releases the diaphragm containing 4 piezoresistors for 1 hour. The etchant #C is maintained at 70℃. The post etching process is depicted in Fig. 6.

Table 1: Recipes of post etchings for CMOS sensors

	Metal	Etchant	Recipe
#A	Ti-W alloy	H_2SO_4:H_2O_2	3:1
#B	Aluminum	H_3PO_4:HNO_3:CH_3COOH:H_2O	14:1:2:3
#C	Silicon	KOH	30%

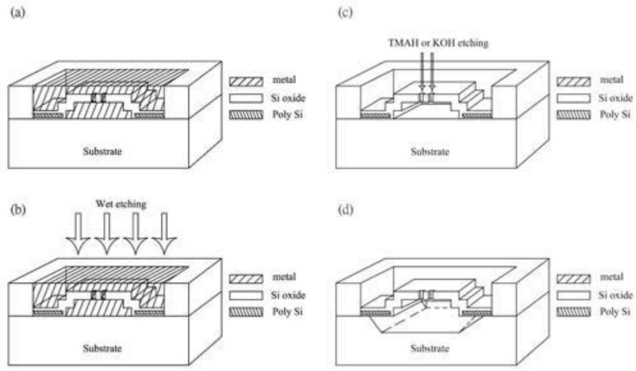

Fig. 6: Post process flow: (a-b) Using the etchants of Table 1 alternatively to remove the composite metal layers; (c-d) Using KOH to etch silicon substrate from front-side and release the poly-Si piezoresistors.

The post etching stops on <111> planes automatically, and forms a pressure cavity with an inverted pyramid configuration. Therefore the lateral dimension of the pressure cavity never gets larger than the sensing diaphragm and the diagonal line of pyramid bottom is defined by the diagonal line of an X-shape sacrificial layer. As a matter of course, this new post process guarantees the dimension of pressure cavities (formed by front-side etching) much smaller than the ones formed by backside etching. Fig. 7

show the SEM photos of a diaphragm: top two photos are the released SiO_2 diaphragm and its etching holes. After the diaphragm is damaged by a microprobe, the V-groove cavity and the residual polysilicon piezoresistors can be confirmed in lower two photos. These pictures show that front-side etching can release the diaphragm structure composing of four resistors without damaging, and the undercut of an X-shape etching window made by sacrificial layer with same configuration leads to a perfect result.

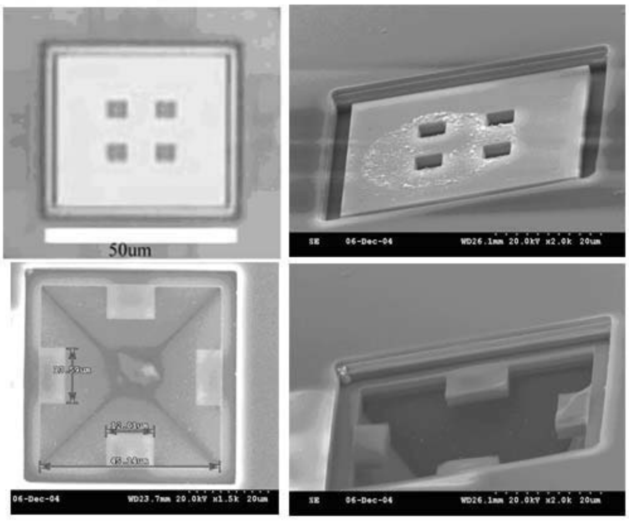

Fig. 7: SEM photo of a released diaphragm

Gelatin sealing material

We still package the pressure sensor by the wire-bonding and cavity sealing before testing. For ensuring the well function of the CMOS pressure sensor, we must seal etching holes on the diaphragm after the post etching to isolate the cavity from the ambient environment. We use a reversible thermoplastic protein, gelatin [6], to seal the etching holes herein. The hydrous gelatin powder can be dissolved in 40℃ water, and becomes consolidation below 25℃. We spin-coat gelatin gel on our CMOS sensor chip, and the gel fills the pressure cavities immediately and automatically. The thickness of a gelatin layer is varied with a concentration of gelatin solution and rotation rate of spin-coater. The recipe of the gelatin solution is 5 wt% and the rotation speed of the spin-coater is 1000 rpm. The surplus gelatin will be flung away to keep the uniformity of a diaphragm. The filled gelatin degrades the output sensitivity of our pressure sensor to a very little extent since the Young's modulus of gelatin is below 1MPa (much smaller than SiO_2: 60GPa.) In other words, the role of filled gelatin in the pressure cavity is like air, but it really meets the sealing requirement of pressure sensors in this work. Fig. 8 shows the photos of sensor packaged with gelatin.

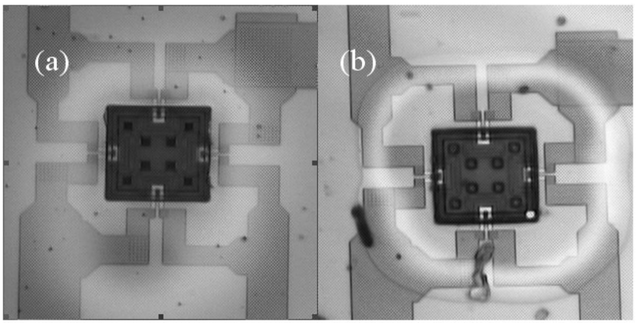

Fig. 8: Gelatin fill-in packaging process: (a) before the sealing process; (b) after the sealing process.

4. EXPERIMENT AND DISSCUSION

We utilize a pressure-testing machine [7] to verify the performance of a completed CMOS sensor. This machine shown in Fig. 9 can control the pressure from 0 to 300 psi and temperature from ambient to 200℃ in a testing chamber. In this research, we fix the temperature at 25℃ and change the pressure from 0 to 60 psi slowly.

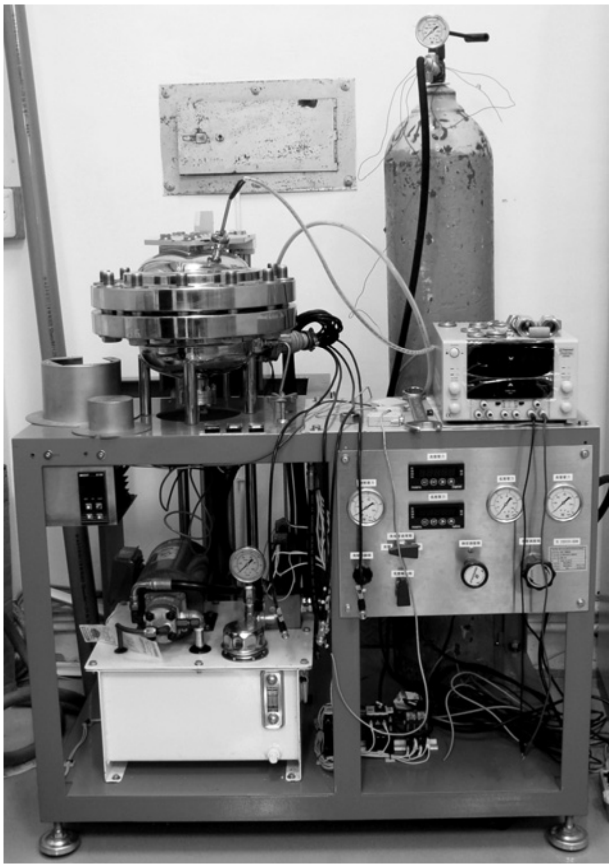

Fig. 9: Pressure testing machine

The experiment setup is shown in Fig. 10. We use a power supply providing a 1 volt DC bias and a data gathering system with a computer to record the output signal. We test the sensor every week for 3 times to realize the performance of the sensor and ensure its reliability. The sensor is placed in the clean room during the testing period.

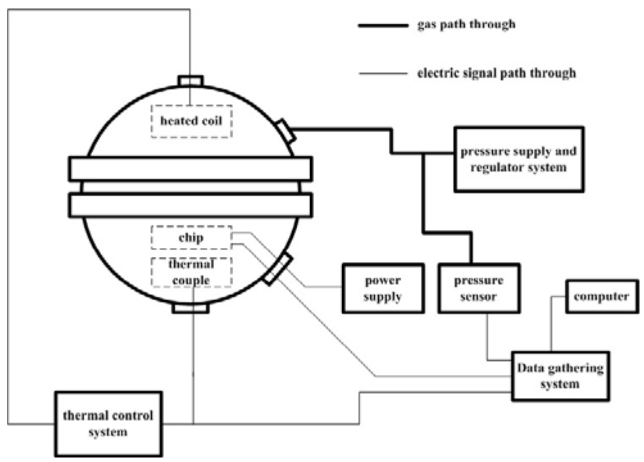

Fig. 10: Sketch of the experiment setup

The output voltage of a CMOS pressure sensor is shown in Table 2 and Fig. 11. The sensitivity is 8.56±0.13mV/V/psi, the non-linearity is 4.3±1.6%, and the hysteresis is less than 1%. The output signals were recorded every week for 3 times. As shown in Fig. 11, these three testing curves are almost identical. It proves that the sensor has a good reliability.

Table 2: Performance of CMOS pressure sensor

NO.	Pressure operation	Sensitivity (mV/V/psi)	Non-Linearity (%)	Hysteresis (%)
1st measure	increase	8.515	3.964	0.716
	decrease	8.517	3.185	
2nd measure	increase	8.463	5.736	0.118
	decrease	8.442	5.906	
3rd measure	increase	8.681	2.848	0.12
	decrease	8.685	2.744	

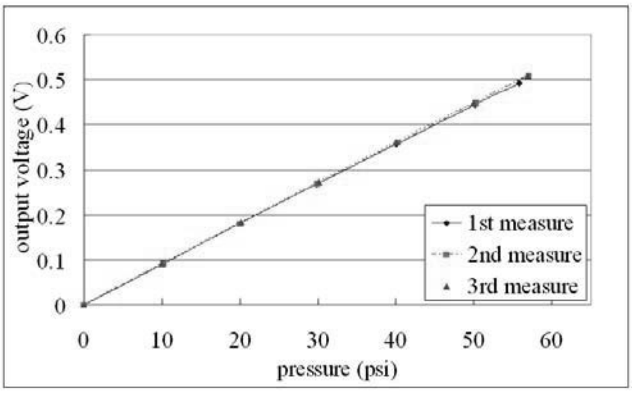

Fig. 11: Pressure testing of a CMOS pressure sensor

The comparison of our CMOS pressure sensor to other previous works is shown in Table 3. Lai's pressure sensor [2] and the sensor this work are piezoresistive, and Chavan's [8] and Salo's [9] pressure sensor are capacitive. In this work, the size of a diaphragm of a sensor is 50× 50μm^2 and it is much smaller than Lai's sensor dimension of 450× 450μm^2. The sensitivity of our sensor is better than Lai's sensor with one order of magnitude, and the non-linearity is superior, too. Although the capacitive pressure sensors have higher sensitivity than piezoresistive one, the linearity of capacitive pressure sensor is worse than the piezoresistive one in general. Even the output sensitivity of Chavan's sensor seems to be better, but the diaphragm or sensor size is not as small as the ones in this work. Basically, we demonstrated a good job of making a very small pressure sensor without degenerating its output performance by a commercial CMOS foundry and a simple post process.

Table 3: Comparison of different CMOS pressure sensor

Inventors	Diaphragm size (μm)	Sensor size(mm)	Sensitivity	Non-linearity
C.-C. Lai [8]	450 × 450 (4μm thick)	1.94×4.05	0.89 (mV/V/psi)	6%
	450 × 450 (24μm thick)	1.94×4.05	3.61×10^{-2} (mV/V/psi)	11%
A.V. Chavan [9]	Diameter 1000~1100 (4μm thick)	6.5×7.5	2.53±0.13 (V/psi)	—
T. Salo [2]	90~150 (3μm thick)	—	26.89 (nm/psi)	—
This work	50 × 50 (2.4μm thick)	3×3	8.56±0.13 (mV/V/psi)	4.3±1.6 %

5. CONCLUSION

In this work, we utilize CMOS foundry and novel post process to fabricate a 50× 50μm^2 piezoresistive pressure sensor with good performance successfully. We used new concepts of the X-shape sacrificial layers, non-planar diaphragm structure and sealing gelatin to complete front-side etching process and to reach the goal of size reducing. The sensor is experimentally demonstrated to be much smaller but still prettily sensitive. Such a small and sensitive piezoresistive CMOS pressure sensor is believed to be useful in monitoring the small-size biological activities in the future.

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