Aligned carbon nanotubes for through-wafer interconnects

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Through-wafer interconnects by aligned carbon nanotube for three-dimensional stack integrated chip packaging applications have been reported in this letter. Two silicon wafers are bonded together by tetra-ethyl-ortho-silicate. The top wafer (100 μm thick) with patterned through-holes allows carbon nanotubes to grow vertically from the catalyst layer (Fe) on the bottom wafer. By using thermal chemical vapor deposition technique, the authors have demonstrated the capability of growing aligned carbon nanotube bundles with an average length of 140 μm and a diameter of 30 μm from the through holes. The resistivity of the bundles is measured to be 0.0097 Ω cm by using a nanomanipulator. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2759989]

Through-wafer interconnects have been proven to be a promising technology to fabricate the next generation three-dimensional (3D) electronic devices or multichip modules.[1–3] Compared to the conventional interconnect technologies, through-wafer interconnects allow signal access from the back side of the devices. By using this method, devices can be assembled together in two dimensions without the packaging gap, which results in the least parasitic losses, resistance-capacitance delay, flight time, and hence, the fastest possible response.[4]

A number of integrated circuit (IC) devices are interconnected in the vertical axis by through-wafer vials filled with copper or other conductive materials. Ji *et al.*[5] reported through-wafer interconnects by filling polycrystalline silicon into etched holes. However, the interconnects have relatively high electrical resistance (~240 Ω) and low aspect ratio (~6). Recently, Dixit and Miao[1] reported high aspect ratio (~15) through-wafer copper interconnect columns, which were fabricated by electroplating and have an electrical resistivity of 2.2 $\mu\Omega$ cm. However, the electromigration of Cu at high current densities (10^6 A/cm^2) is a critical problem in interconnects for high performance electronic applications.[6] Other challenges include increasing oxidation resistance and preventing the diffusion of copper into silicon substrate.

In this regard, carbon nanotube becomes an ideal candidate material for electrical interconnects due to its extraordinary electrical, mechanical, and thermal properties.[7] Wei *et al.*[8] showed that, at 250 °C, the current carrying capacity of multiwalled carbon nanotubes (MWCNTs) did not degrade even after 334 h with current densities of 10^{10} A/cm^2. The mechanical properties of CNTs are also superior to those of conventional packaging materials used in the current IC industry.

Growing MWCNTs inside vias with a diameter of 400 nm (~1.25 μm depth) was reported by Kreupl *et al.*[9] Li *et al.*[6] also reported a bottom up CNT growing approach. In his work, MWCNTs (~1.5 μm long) are first grown at prespecified locations, and the free gap between individual CNT is filled with SiO_2 by chemical vapor deposition (CVD) using TEOS. This is followed by chemical mechanical polishing to remove the excess SiO_2. Both research groups have shown interesting works, yet the effective lengths of CNTs are quite short, which is a limitation for the 3D through-wafer IC packaging.

Zhu *et al.*[10] demonstrated a reproducible process for the growth of CNT bundles up to 400 μm with an aspect ratio of 32. These impressive results proved the possibility of growing long CNTs with high aspect ratio. However, the CNTs synthesized by them were standing freely on the silicon surface and not grown from the through holes; in other words, real through-wafer interconnects by using the high aspect ratio CNT bundles had not been accomplished yet.

We provide an alternative and a viable solution for through-wafer interconnects. Two wafers are bonded together, and CNT bundles are uniformly grown from the bottom wafer through the holes patterned in the top one. By this method, the length of the CNT can be well controlled by the increasing growth times and different sample orientations. Two silicon ⟨100⟩ wafers are used and four main steps are included in the fabrication process. In the first step, through holes with diameter ranging from 30 to 60 μm are created by deep reactive iron etching[11] (DRIE) in the top wafer (100 μm thick). A thin sol-gel tetra-ethyl-ortho-silicate (TEOS) film serves as a bonding layer[12] (~100 nm thick) and it is deposited onto the top wafer after the DRIE. Secondly, an iron catalyst (2 nm thick) film is deposited onto the bottom wafer (350 μm thick with 500 nm thick thermal oxide) by electron beam evaporator. Thirdly, two wafers are bonded together through the use of a bonding machine (SUSS SB6) at 400 °C. Finally, the bonded wafers are cut into small samples (5×5 cm^2) and placed in a 4 in. barrel quartz tube to grow CNT via thermal CVD.

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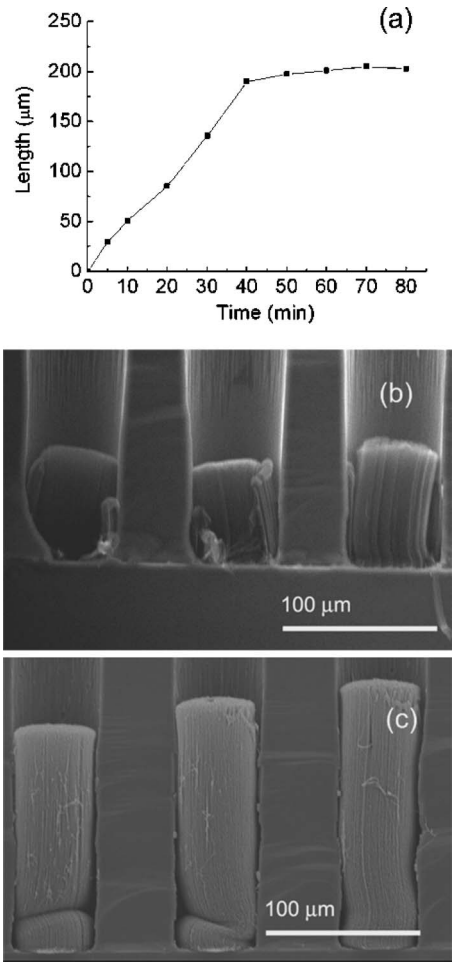

FIG. 1. Images of (a) the relationship between the CNT length and the growing time at 700 °C. SEM images for CNTs grown in through holes with (b) samples with vertical orientation and (c) samples with slant orientation.

During the CNT growing process, hydrogen (H_2), acetylene (C_2H_2), and argon (Ar) are used as process gases and CNTs grow at temperatures between 490 and 900 °C in our studies. The results presented here are obtained at 700 °C. In the first stage, H_2 [10–100 SCCM (SCCM denotes cubic centimeter per minute at STP)] and Ar (40–400 SCCM) are released into the quartz tube. Then the heater is turned on. As temperature reaches 700 °C, the samples are soaked for 15 min. After that, C_2H_2 (100 SCCM) is turned on for 5–80 min. The annealing process is executed for 5 min after the C_2H_2 gas is turned off. Samples are taken out after the quartz tube is cooled down to the room temperature.

In order to synthesize through-wafer CNTs, one of the most challenging tasks is to grow long enough CNTs to connect the bottom wafer to the top bonded wafer. The growing time and sample orientation are found to be the two dominant factors that affect the length of CNT. Figure 1(a) shows the relationship between CNT length and growing time at 700 °C. The length of CNTs increases rapidly from 30 to 190 μm in the first 40 min, but eventually levels off at about 200 μm for long growing durations. This phenomenon has also been observed in many thermal CVD processes.[13–15]

The second factor that affects the CNT growth length is the sample orientation places in the quartz tube. Under the same synthesis conditions, the samples are placed horizontally, vertically, and slantwise. In the horizontal position, through holes are perpendicular to the direction of gas flow, while in the other two positions, through holes are placed toward the direction of gas flow. There are very few CNTs grown in horizontal position. The lengths of such CNTs are observed to be very short (~4 μm long). However, long CNT bundles are observed in the holes under vertical and slant positions. The scanning electron microscope (SEM) images of the synthesized CNT bundles are shown in Figs. 1(b) and 1(c). The lengths of the CNT bundles are about 70 and 180 μm for vertical and slant positions, respectively.

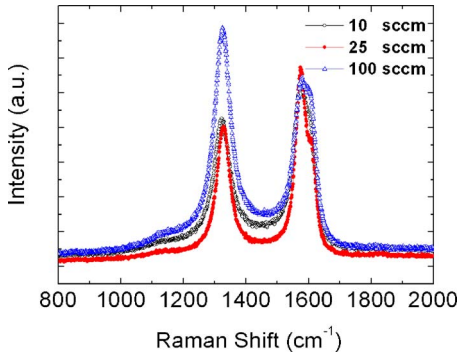

FIG. 2. (Color online) Raman spectrum of CNTs synthesized with flow rate of 10, 25, and 100 SCCM, respectively.

Raman spectroscopy (Renishaw Raman Microprobe-RM1000, 633 nm excitation wavelength) is used to characterize the graphitic ordering of the grown CNTs at gas (C_2H_2) flow rate from 10 to 100 SCCM. The spectrum shown in Fig. 2 displays a strong *G* band at 1578 cm^{-1} and weak *D* band at 1326 cm^{-1}, which are similar to that reported by Li *et al.*[16] and Dresselhaus and Dresselhaus.[17] The maximum intensity ratio (I_G/I_D) is achieved at a flow rate of 25 SCCM. These results indicate that CNTs with highly ordered graphitic tubular structures are produced at this flow rate. The I_G/I_D ratio decreases at flow rates of 10 and 100 SCCM. *D* band value is higher than that of *G* band at the flow rate of 100 SCCM. This suggests that some defectives such as nanocarbon materials are generated in the structure. One of the possible causes of the higher density of the *D* band is due to the relatively lower synthesis temperature at 700 °C.[13]

Figure 3(a) is the top view of the SEM image of the CNT bundles grown in the two bonded wafers. The average diameter of the CNT bundles shown in the figure is 50 μm with a pitch of 110 μm. The image clearly shows that the CNTs grow out of the top wafer (100 μm thick). The CNT bundles with a diameter of 30 μm can also grow out of the top wafer. The detailed view of two CNT bundles is shown in Fig. 3(b). It can be seen that the CNTs are well aligned without any disorientation. A high magnification SEM image of the CNT bundle is shown in Fig. 3(c). The diameter of the single CNT varies from 30 to 130 nm and the estimated CNT density could reach about 70/μm^2.

I-V characterization of the CNT bundle is carried out by using a nanomanipulator. As shown in the test setup in Fig. 4(a), a CNT bundle is laterally placed on an insulating substrate. One probe is contacted at one end of the CNT bundle while another embeds into the bundle near to the other end. The length between the two contact points is about 81 μm. The current-voltage (*I-V*) characteristic is shown in Fig. 4(b). An almost linear relationship is observed between current

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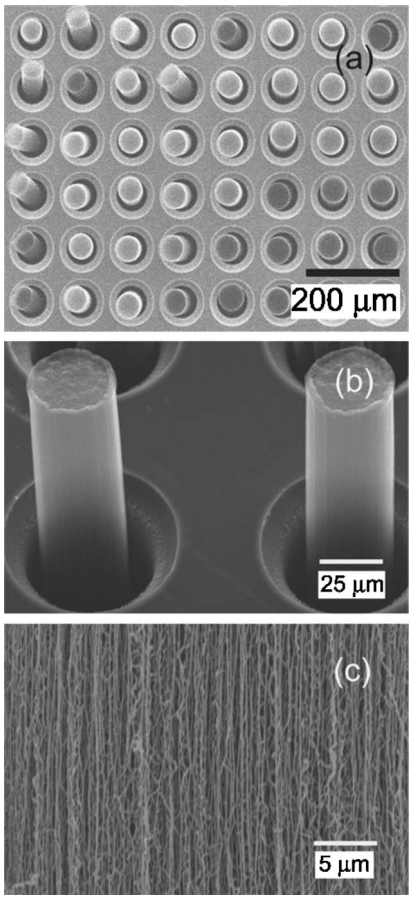

FIG. 3. SEM images for CNTs grown out of the top bonded wafer. (a) Overview of CNT bundles. (b) Detailed view of two CNT bundles taken with an angle of 45°. (c) A high magnification SEM image of the CNT bundle.

and voltage, and this reveals that CNT bundle is of metallic nature. Under the same characterizing condition, the electrical resistance in a direction vertical to the bundle axis is also measured and the value is found to be much larger than that parallel to the bundle axis. This result is in agreement with that report by Wang *et al.*[18] The average electrical resistance shown in Fig. 4(b) is about 2 kΩ, which is equivalent to an estimated resistivity of 0.0097 Ω cm considering the effective contact area between probes and CNT bundles. This value is slightly higher than the reported value by Song *et al.*[19] (~0.0065 Ω cm) and Dai *et al.*[20] ($8\times10^{-4}-12\times10^{-3}$ Ω cm) due to the test methods. First, the CNT bundle is directly contacted by probes. Although the contact resistance is not clearly indicated in the current-voltage characteristics, it definitely increases the electrical resistance. Second, the probes contacted only on the sidewalls of the CNTs during the measurements, and this also results in a higher electrical resistance. The measured electrical resistance will be reduced if the probes are well contacted with the ends of the CNT bundle. Although the measured electrical resistivity is orders of magnitude higher than that of copper interconnect by electroplating[1] and is still too large for direct CNT interconnect applications, the through-wafer CNT bundles synthesized in this work exhibits a promising solution for advanced electrical interconnects.

In conclusion, we have demonstrated a reproducible and reliable process to synthesize high quality CNT bundles through bonded wafers with through holes at 700 °C by thermal CVD process. The average length of the CNT bundle is 140 μm with a minimum diameter of 30 μm. This is sufficient for most of the through-wafer interconnect applications. The preliminary results achieved in this study provide a promising solution to integrate CNTs into multilevel interconnects, to meet the future needs of 3D IC packaging.

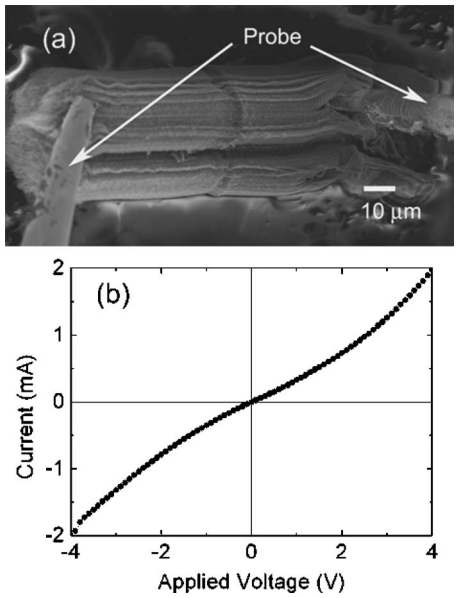

FIG. 4. Images of (a) two probe measurement setup in nanomanipulator taken by SEM. (b) *I-V* curve of the CNT bundle.

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